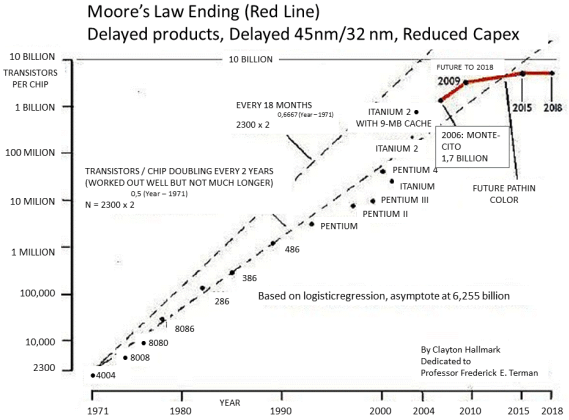
Using carbon nanostructures as the assembly platform in semiconductor advanced packaging beyond Moore

INTRODUCTION:

Industry trends

Moore's law has guided the ever continuing miniaturization and performance enhancements of silicon chips for the semiconductor industry by scaling the transistor size. After 50 years the industry is now witnessing a paradigm shift.



In a series of articles published very recently [1, 2, 3, 4, 5] one may observe a number of trends. One observation is that the industry is now moving from the unique consensus driven evolution of the past to "no consensus" where no roadmap as such is present. It is also evident that application driven evolution is replacing transistor scaling driven evolution. In the digital circuit world, reprogrammable chips are becoming more prominent over the static chips and 2D integration is shifting to more desirable 2.5D and 3D stacking to reduce the overall footprint and cost. And last but not least, chip making is shifting to comply with the strong needs of self-containability that is driven by Internet of Things (IoT).

The bottom line is that there is a strong need for a technological shift from the trend of scaling the transistors to the reduction of the size of electronic package.

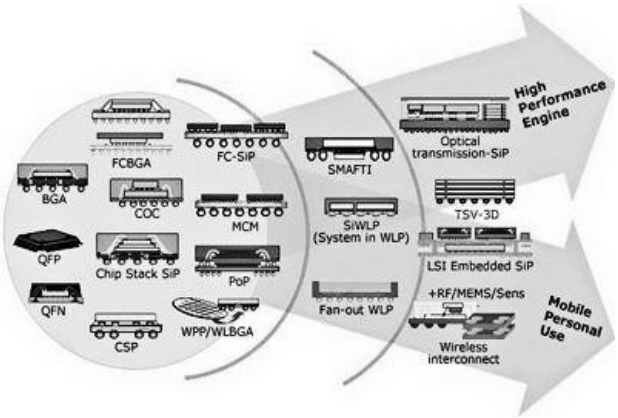
The need for a technology shift

According to Dr. Samueli, co-founder and chairman of Broadcom, "The cost-effectiveness seems to have hit a sweet spot at about 28nm" [4]. To gain significant cost and performance benefits from shrinking further, it is necessary to improve the technology around electronic packaging solutions such as System on Chip (SoC) or System in Package (SiP) which leads to the need for an advanced wafer level packaging platform [5].

> *"The semiconductor industry will soon abandon its pursuit of Moore's law. Now things could get a lot more interesting."*
>
> *M. Mitchell Waldrop, feature editor, Nature, 09 February 2016: "The chips are down for Moore's law"*

Companies like Apple are willing to pay a premium cost to shrink the overall size of the package further in order to gain crucial millimeters and make their phones slimmer and more elegant [4]. However, the scaling of electronic packaging faces the bottleneck when it comes to shrink the size of the metal pillars/interconnects.

The superiority of carbon nanostructures is well known but growth temperatures has prevented industrial integration.



IC packaging evolution and roadmap (Courtesy: Reneseas Electronics)

Today, the existing well established technologies struggle to go down in dimension in x, y and z without compromising the cost and power performance.

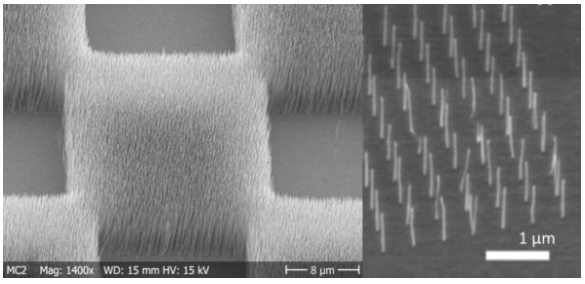
CORE TECHNOLOGY

Background

Smoltek's journey started in 2005 with the ambition to develop a viable process to enable growing of carbon nanostructures on a CMOS industrial platform at industry compatible temperatures; with an initial target to reach a growth temperature at 450°C.

Controlled growth on a substrate using CVD

The growth related inventions over the years constitute three different paths to fulfill several technological aspects and together define the core technology. In brief, inventions cover combinations of material stacks that enable to grow nanostructures on different substrates and the freedom to tailor the positioning and properties of the grown nanostructures.



Left: nanostructures grown in "checker box" pattern
Right: an array of nanostructures grown on a substrate

Controlling morphology and electrical properties

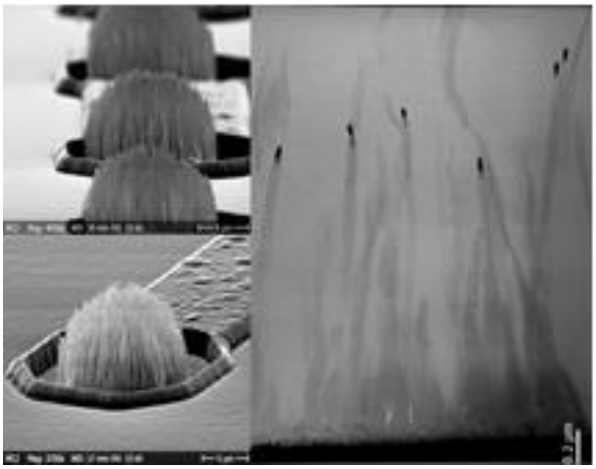
Typically, the growth with a CVD method is a catalyst driven process. One aspect of the invention is to allow one extra control layer apart from the catalyst layer to interact chemically in order to enable the growth. This small trick in introducing the control layer is the pivot to provide an engineering parameter platform that can be tuned to control and optimize the properties of the nanostructures to specific requirements. Allowing for a certain degree of interdiffusion enables control over the morphology of the grown nanostructures and the electrical properties of the interface between the nanostructures and the substrate.

Protecting the passive and active devices on the bottom surface

Another aspect of the core technology is the "help layer" that prevents the bottom surface with active and passive devices from being damaged during a growth process. Such a help layer becomes essential to grow nanostructures on an insulating substrate or on a confined area that needs to be protected during the CVD growth processes.

Controlling the interaction between layers

The third extension of the core technology brings the flexibility to tailor and impact the growth mechanism through having a mismatch of "grain layer" distributions of the catalyst layer and the layer to grow on. Such control enables interactions between the layers and hence the growth parameters and the properties of grown nanostructures.



Left: nanostructure bumps grown from Al metal pads
Right: cross section electron microscope confirming excellent solder wetting with no void formations

Summary: The core technology involves depositing one or more layers on a substrate in order to engineer the growth of nanostructures to specifications and/or to protect the underlying device layer or the combination thereof. The process has so far proven to work down to 375°C making it compatible with CMOS compliant materials and processes.

APPLICATIONS

Once the growth of a nanostructure is feasible on an industrial platform, it is possible to exploit the properties of grown nanostructures for different applications. At Smoltek we have already innovated a number of demonstrators and now encourages others to do the same.

Smoltek Application Demonstrators

Based on the core nanostructure growth technology Smoltek has demonstrated the following applications and functional properties by utilizing CNF's for:

Semiconductor Advanced Packaging applications – integrated on device, interposer or carrier:

- ultra-fine flip-chip bump interconnects
- mini super-capacitor for energy storage, filtering or decoupling
- RF device interconnects
- die attach films for thermal, electrical and/or mechanical purpose

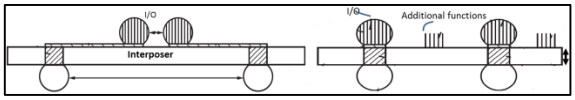
Electronic components:

- electrochemical or solid-state mini super-capacitors

General properties demonstrated:

- ✓ interconnects with ohmic behavior
- ✓ high RF power drive capability
- ✓ field emission properties at a very low voltage - can be used as high definition electron emitters
- ✓ selective electroplating possible based on conductive properties
- ✓ solid solder-wetted - without voids at the joints, suitable for flip chip interconnects
- ✓ conformal insulator coating can be applied
- ✓ can be embedded in composites with polymer, wax, and metallic composite (CNF+plated metal, CNF+Pbfree Solder)
- ✓ mechanical properties for high aspect ratio nanoimprint stamp for pattern transfer
- ✓ die bonding to standard lead-frame, shear strength compliant with MILx1 standard using polymer adhesive

SMOLTEK Tiger™ - the game changer



SMOLTEK Tiger™ is a carbon nanostructure based assembly platform targeting the next wave of advanced packaging that:

- offers 3D-shrinkage of orders of magnitude (>10x-100x) compared to existing and well established bump/pillar technologies, hence will enable to fully unleash the full power of semiconductor miniaturization.
- is simple and primarily utilizes arrays of metallic pillars enabled by nano-structures that make it suitable to mount bare dies stacked on each other or bonded to a substrate (interposer) or carrier (lead-frame).
- can be extended to include technology to embed additional functionality e.g. energy storage (solid state supercap) to offer a complete self-sustained package with tailored energy density and life time.
- enables integration of standard ICs, ASICs, FPGAs, µ-controller, memory, etc. to be configured according to the need of the end user design.

"When we moved from transistors to integrated circuits, we shrunk an entire rack measuring about 40 cubic feet down to a single board measuring 19 x 26 inches. 3D stacking will shrink that board down to less than a square inch and we can potentially get an increase in power performance of at least 10-100 fold."

Bernie Meyerson, IBM's Chief Innovation Officer, Forbes, 24 February 2016: "How IBM Plans To Innovate Past Moore's Law"

With SMOLTEK Tiger™ the semiconductor advanced packaging industry can fulfill the need for performance boost, higher functional integration and smaller package size at an attractive cost to performance ratio for product evolution beyond Moore.

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