

(19)



(11)

EP 2 197 782 B1

(12)

EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
04.03.2020 Bulletin 2020/10

(51) Int Cl.:
B82B 1/00 ^(2006.01) **B82B 3/00** ^(2006.01)
H01L 21/60 ^(2006.01) **H01L 23/488** ^(2006.01)
H01L 23/498 ^(2006.01) **H01L 21/58** ^(2006.01)
C23C 16/22 ^(2006.01)

(21) Application number: **08794128.2**

(22) Date of filing: **10.09.2008**

(86) International application number:
PCT/SE2008/000506

(87) International publication number:
WO 2009/035393 (19.03.2009 Gazette 2009/12)

(54) CONNECTING AND BONDING ADJACENT LAYERS WITH NANOSTRUCTURES

VERBINDEN UND BONDEN VON BENACHBARTEN SCHICHTEN MIT NANOSTRUKTUREN
CONNEXION ET LIAISON DE COUCHES ADJACENTES À L'AIDE DE NANOSTRUCTURES

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MT NL NO PL PT RO SE SI SK TR

(30) Priority: **12.09.2007 US 971859 P**
20.09.2007 US 974045 P

(43) Date of publication of application:
23.06.2010 Bulletin 2010/25

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Description

CLAIM OF PRIORITY

TECHNICAL FIELD

[0001] The technology described herein generally relates to nanostructures, and more particularly relates to use of nanostructures to connect and bond adjacent layers of conductive materials.

BACKGROUND

[0002] There are many instances in the production and manufacture of electronic devices that a layer of material, such as present in one component, is required to be attached - often at specific locations - to a substrate, such as a wafer or die. In such instances, the integrity of the attachment, whether it is mechanically, thermally or electrically, can be critical for the performance of the device.

[0003] Examples include: attaching or bonding a flip-chip to an underlayer (a substrate such as a die); fine-pitch chip-on-flex technology as used in LCD manufacture; and wafer-level bumping for creating electrical contacts at a fine pitch. In all such applications, current technologies are experiencing significant limitations, due in part to the increasing demands for miniaturization of electronic devices.

[0004] use of "flip chip" technology is growing rapidly and the technology is currently used in devices such as mobile phones, MP3-players, smart cards, displays, computer peripherals. However, in terms of complexity and product cost, flip chip technology has drawbacks, due to the requirements of complex processes that involve bonding and connecting the flip chip to the die. These processes include solder flux coating, chip/board arranging, solder bump reflow processes, flux removal processes, underfilling, and cure processes.

[0005] The techniques used in bonding and connecting flip-chips are moving towards increasingly greater numbers of I/O contacts, and finer pitches between the contacts. See, for example, "Anisotropic Conductive Film for Flipchip Applications: An Introduction," by Peter J. Opdahl, available at www.flipchips.com/tutorial05.html, incorporated herein by reference.

[0006] As an alternative to solder bumping, anisotropic conductive film (ACF) has emerged as a lead-free, environmentally-friendly, and flux-less bonding solution consisting of conductive particles dispersed in a polymer matrix, such as an adhesive resin. ACF works by trapping conductive particles between a conductive surface, such as a conductive bump on a flip chip, and another conductive surface, such as a conductive pad on a substrate corresponding to the conductive bump on the flip chip, while insulating adjacent particles from one another.

[0007] During the last few decades, ACF has been widely used for packaging technologies in the flat panel display industry to make electrical and mechanical con-

nections from an integrated circuit driver to a glass substrate in a display. Lately, ACF has proven to be a popular alternative to other direct chip-attach technologies, in order to satisfy requirements of finer pitch at lower dimensions. For the ACF material this means making the conductive particles as small as possible, creating high particle density, and ensuring extremely evenly distributed particles within the ACF. In addition, the flow of the polymer matrix typically has to be as well-controlled as possible. Currently, particles as small as 3.5 μm in size are used in demanding applications.

[0008] It has long been recognized that ACF suffers from a number of limitations. If the particles are too large, or if there are too many particles, there is a risk of creating a short circuit between two neighboring bumps on the flip chip. This means that there are limitations on the minimum possible pitch between particles, since a short-circuit can arise if the particles are too close to each other. This is particularly evident in, e.g., the display industry, where black dots will appear when a short-circuit occurs. As there is no clear way of predicting with precision the uniformity of particle distribution within the polymer matrix, the risk of short-circuiting is always present. The impact of avoiding the risk of short-circuiting due to the particles is that the maximum possible number of contacts (I/O's) is limited, and thus the maximum possible pitch is limited when connecting a flip-chip using ACF.

[0009] Chip On Flex (COF), is a related technology that also utilizes ACF, and triggers similar issues to "flip-chip" technologies as the demand (particularly in the LCD industry) increases for finer pitch products (less than the 40 - 50 μm in current products) in order to meet cost and size requirements. There are two main issues in fine-pitch COF packaging that arise with the current bonding process: lead breakage and misalignment.

[0010] Since lead breakage during the assembly process can happen at any instance, and at any position, a visual inspection is almost impossible. Lead breakage can occur when there is a lack of trapped conductive particles between the two conductive surfaces; a trapped particle count less than one creates a high probability of an open electrical connection, which leads to electrical failure. In order to avoid that problem, the particle density must be increased, which is accomplished by reducing the diameter of the particles. If the lead pitch of the COF is 40 μm , an anisotropic conductive adhesive (ACA) with a particle diameter of less than 3 μm can be employed to achieve 99.95% chance of a good electrical connection (at least one trapped particle).

[0011] However, even at that high rate of connection integrity, the margin of error cannot be ignored. For example, for packages with 400 bumps, one out of five chips may have an open (disconnected) bump/lead joint. Moreover, if the magnitude of gap variation between bumps and leads exceeds 3 μm , an open joint failure can occur even with normal joints with trapped particles. Therefore, overall, the application of an anisotropic conducting adhesive (ACA) to fine-pitch COF interconnection requires

reduced particle size and more accurate control of bump/lead height and chip/film coplanarity.

[0012] Misalignment also becomes a greater risk at finer lead pitches, since finer pitches require higher-precision control over the alignment between the film and the conductive surfaces. The existing tolerance requirement eventually needs to be replaced with a new standard for satisfactory yields. The causes of misalignment in the COF assembly process are various and may be in the film, chip, bonding equipment, and so on. The bonding tolerance relates to the nature of variation.

[0013] Thus, the main problems with ACF can be summed up as: (1) the need for uniform distributed particle size; (2) the need for control of bonding pressure to break the surface coatings of the particles and to create contacts; (3) limitations in size of the particles with respect to distribution of particles - one cannot go down to sub micron level; and (4) manufacturing limitations - one cannot manufacture at the sub micron level with good and reproducible uniformity. Accordingly, there is a need for a better way of forming connections between a chip and a substrate and of attaching a chip to a substrate. In this context, US 2006/243958 discloses an anisotropic conductive film (ACF) including a plurality of carbon nanotubes (CNTs) embedded in a cured polymer layer. US 2004/182600 discloses electronic device having a structure of an ohmic connection to a carbon element cylindrical structure body.

[0014] Wafer-level bumping is subject to similar considerations. The need for "bumps" for creation of the electrical contacts through distribution or contact channels with lower dimension and finer pitch demands ever greater fidelity of manufacture. Electrical connections are created by bumps, but there are limitations in the size of those bumps; it is not possible to go down to sub micron level with current manufacturing processes, which are constrained in the number of bumps per unit area. Thus, a number of distribution channels are suffering from the constraints of creating the bumps.

[0015] The discussion of the background herein is included to explain the context of the technology. This is not to be taken as an admission that any of the material referred to was published, known, or part of the common general knowledge as at the priority date of any of the claims found appended hereto.

[0016] Throughout the description and claims of the specification the word "comprise" and variations thereof, such as "comprising" and "comprises", is not intended to exclude other additives, components, integers or steps.

SUMMARY

[0017] The object underlying the present invention is achieved by a bonding film according to claim 1. Any embodiment not comprising all the features of claim 1 does not pertain to the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018]

5 FIG. 1: bonding and electrical contacting of a die to a substrate using carbon nanofibers in a matrix - principle.

FIG. 2: bonding and electrical contacting of a die to a substrate using carbon nanofibers in a matrix, prior to curing.

10 FIGs. 3A, 3B: bonding and electrical contacting of a die to a substrate using carbon nanofibers in a matrix, after curing.

FIG. 4: Top view of carbon nanofibers in a matrix.

15 FIG. 5: Top view of carbon nanofibers in a matrix with an I/O pad.

FIG. 6: Cross-sectional view of carbon nanofibers in a matrix with an I/O pad.

FIG. 7 shows a flow-chart of a process as described herein;

20 FIG. 8 shows a flow-chart of a process as described herein; and

FIG. 9 shows a flow-chart of a process as described herein.

DETAILED DESCRIPTION

[0019] The instant technology is directed to methods of connecting two surfaces or layers by bonding nanostructures to contact locations on the two surfaces or layers, thereby creating mechanical, electrical, or thermal connections between the two surfaces or layers. By such methods, the pitch of the contact locations may be within the inclusive range of 2 nm to 1 mm. The instant technology further includes an apparatus comprising a first conductive surface or layer, a second conductive surface or layer, and a nanostructure assembly bonded to and positioned in between the two conductive surfaces or layers, such that the nanostructures of the nanostructure assembly are oriented perpendicular to the two conductive surfaces or layers.

[0020] In other aspects of the technology, a bonding layer is formed by growing nanostructure, such as carbon nanostructures (CNS), on metallic underlayers formed on a substrate. The substrate may comprise one or more layers of metal, semiconductive materials, or insulating materials, or combinations thereof. The nanostructures grow perpendicular to the substrate surface. The nanostructures can be coated in a carrier such as a polymer, e.g., an adhesive polymer. The carrier may be a polyimide, or may be a flexible or solid material. Optionally the nanostructures, coated or not, can be polished to provide uniform length. The resulting structures can be diced into individual films. Optionally, the film of polymer and nanostructures can be lifted from the substrate. The film can then be applied to the surface of a die to provide wafer contacts.

[0021] In still other aspects of the technology, a wafer

bonding layer includes nanostructures, such as carbon nanostructures (CNS), held in a polymer coating. The nanostructures extend perpendicularly to the top and bottom surfaces of the layer. The nanostructures can be grouped, with nanostructures within a group at a regular spacing, and groups at another regular (larger) spacing. Nanostructures within a group can be electrically connected, either by being placed in direct contact with a common electrode, or by being grown on metal underlayers that are electrically coupled. In contrast, nanostructures of separate groups are electrically isolated.

[0022] When "perpendicular" is used herein to describe an orientation between a nanostructure and a layer or surface, it is understood that the nanostructure is of the form of a wire, tube, or fiber, or similar structure, that has a longitudinal axis extending along its length, and it is the longitudinal axis that is disposed normal to the plane of a layer or surface. It is further to be understood that "perpendicular" encompasses small deviations from exact perpendicularity, such as for example an inclination of the longitudinal axis that is 88 - 90° with respect to the plane, or 85 - 90° with the respect to the plane.

[0023] In some embodiments, the nanostructures are generally rigid, such that the layer that contains them can be generally incompressible.

[0024] Examples of nanostructures include, but are not limited to, nanotubes, nanofibers, or nanowires. In particular, nanostructures found herein can be made of carbon based nanostructures such as carbon nanotube(s), carbon nanofiber(s), or carbon nanowire(s).

[0025] Nanostructures found herein can also be made of other materials such as metals, III-V, II-VI compounds, or combinations of elements from the periodic table of the elements. Examples of materials include semiconductors such as GaAs, InP, InGaAs, AlGaAs, nanowires such as silicon nanowires, alloys such as ZnO, ZnAlO, and any other binary or ternary alloys from which nanostructures can be formed.

[0026] Nanostructures consistent with applications herein can be grown/formed/deposited on substrates such as silicon, polysilicon, oxidized silicon, silicon nitride, germanium, silicon-germanium, GaAs, AlGaAs, GaN, InP, glass, polyimide, polymer, metals such as W, Mo, Ti, Cr, NiCr, Al, AlOx, Pt, Pd, Au, Cu, TiN, or any other metal from the periodic table, plastics, aluminium foil, alumina, papers, and high k materials such as HfO, ZrO, etc. For growth of the nanostructures, the catalyst can be of Ni, NiCr, Pd, Pt, Fe, Au, Co, or combinations of such metals, or alloys of different materials, for example bimetallic catalysts such as Co-V, Co-Ni, Fe-Ni, etc.

[0027] Chemical Vapor Deposition (CVD) is a typical method for growth of nanostructures for use with the technology described herein. However, there are different kinds of CVD methods that can be used, e.g., thermal CVD, PECVD, RPECVD, MOCVD (metallo-organic CVD), etc. or any other variants of CVD as is known by the skilled artisan. Particular methods of growth are described in U.S. Pat. Appl. Ser. No. 11/412,060, "Control-

led Growth of a Nanostructure on a Substrate," filed April 25, 2006, which is incorporated herein by reference in its entirety.

[0028] Still further, the nanostructures herein can be formed from methods and materials, employing conditions, that permit control of various properties of the nanostructures once formed. Thus, the nanostructures used herein encompass nanostructures grown from substrates, and interface layers situated therebetween, having the following characteristics. The substrate is preferably a conducting layer such as a metal layer, which may be disposed on a support. The support is typically a wafer of silicon or other semiconducting material, glass, or suitable flexible polymer used in thin film technology. The metal is preferably selected from the group consisting of molybdenum, tungsten, platinum, palladium, and tantalum. The thickness of the metal layer is preferably in the range 1 nm to 1 μm and even more preferably in the range 1 nm to 50 nm. The metal layer is preferably deposited by any one of several methods known in the art, including but not limited to: evaporative methods such as thermal or vacuum evaporation, molecular beam epitaxy, and electron-beam evaporation; glow-discharge methods such as any of the several forms of sputtering known in the art, and plasma processes such as plasma-enhanced CVD; and chemical processes including gas-phase processes such as chemical vapor deposition, and ion implantation, and liquid-phase processes such as electroplating, and liquid phase epitaxy. Examples of deposition technologies are found in Handbook of Thin Film Deposition, K. Seshan, Ed., Second Edition, (William Andrew, Inc, 2002).

[0029] The interface layers, also called intermediate layers or an intermediate layer, comprise one or more layers, in sequence, disposed upon the substrate. On top of the interface layers is a layer of catalyst. The nanostructure is grown from on top of the catalyst layer.

[0030] The interface layers may consist simply of a single layer of material. In this circumstance, the single layer can be silicon or germanium. The layers can be deposited in amorphous or crystalline forms by techniques such as evaporation, or sputtering. The thickness typically ranges from 1 nm to 1 μm and also in the range 1 nm to 50 nm.

[0031] The interface layers may comprise several layers of different materials and may be, arbitrarily, classified according to function. For example, the layers in the vicinity of the substrate are characterized as layers that influence the electrical properties of the interface. The layers in the vicinity of the catalyst are characterized as layers that influence the composition and properties such as electrical/mechanical properties of the nanostructure.

[0032] Various configurations of interface layers are compatible with the present invention. For example, a sequence of up to 3 layers may be deposited on the substrate, for the purpose of controlling the electrical properties of the interface. Such configurations include, but are not limited to: a sequence of insulator, conductor or semiconductor, and insulator; a sequence of insulator

adjacent to the substrate, and a semiconducting layer; a sequence of semiconductor, insulator, semiconductor; a sequence of two insulating barrier layers adjacent to the substrate, and a semiconductor; a single layer of a metal that is different from the metal of the substrate; and a sequence of a metal that is different from the metal of the substrate, and a semiconducting layer. In such configurations, the insulator may be selected from the group consisting of: SiO_x , Al_2O_3 , ZrO_x , HfO_x , SiN_x , Al_2O_3 , Ta_2O_5 , TiO_2 , and ITO. The semiconductor may be silicon or germanium. The metal, where present, may be palladium, platinum molybdenum or tungsten. Where two layers of the same character are present, e.g., two semiconducting layers, it is not necessary that the layers have the same composition as one another.

[0033] The uppermost layer of the foregoing interface layers may itself abut against the catalyst layer. This is particularly the case where the uppermost layer is a semiconductor such as silicon or germanium. However, it is additionally possible for the foregoing interface layers to have disposed upon them a further layer or sequence of layers that lies between them and the catalyst layer. Such additional, or second, interface layers are thought of as controlling the properties and composition of the nanostructure. The second interface layers may be a pair of layers, such as a metal layer and on top thereof a semiconductor layer adjacent to the catalyst layer. Alternatively, the second interface layers may simply consist of a single layer of semiconductor. The metal layer, where present in the second interface layers, is preferably selected from the group consisting of tungsten, molybdenum, palladium, and platinum. The semiconducting layer in the second interface layers is preferably silicon or germanium.

[0034] The catalyst layer is typically a layer of metal or metal alloy, and may contain very fine particles of metal or metal alloy instead of being a continuous film. The catalyst layer preferably comprises a metal selected from the group consisting of nickel, palladium, iron, nickel-chromium alloy containing nickel and chromium in any proportions, and molybdenum.

[0035] The nanostructures typically have a multi-stack configuration of at least one material layer between the catalyst layer and the conducting substrate, wherein the material is not of the same kind as the catalyst and conducting substrate, and wherein the material controls the chemical reactions between the various layers. Thus, the growth of the nanostructures on different conducting substrates can be controlled. Thereby the morphology and properties of the grown structures as well as the tip materials of the grown structures can be controlled. The current technology can be extended to having several stacks of materials of different kinds (semiconducting, ferroelectric, magnetic, etc.) which can be used to control the properties at base/interface, body and the tip of the nanostructure. It is also possible that the nanostructure is grown upon a conducting layer which is itself deposited on a substrate that itself can be of any kind, such as

conducting, insulating or semiconducting.

[0036] Typically, during growth of such nanostructures, some diffusion of the material of the intermediate layers into the nanostructures occurs. Such interdiffusion may transport the material of the intermediate layers all the way to the tip of the grown nanostructures. In some conditions, the diffused material is present as a narrow band; in others, the diffused material is spread out through the nanostructure.

[0037] The methods described herein are applicable in any assembly techniques for electronic components that include analog and/or digital electronic circuits. For example, such components may be found in: communications engineering, car/industrial electronics goods, consumer electronics, computing, digital signal processing and integrated products. Attaching technologies such as ball grid array (BGA), flip chip (FC) modules, CSP, WLP, FCOB, TCB may utilize the methods herein. Integrated Circuit (IC) types such as RFID, CMOS, BiCMOS, GaAS, AIGAs, MMIC, MCM, may utilize the methods described herein. Display technologies such as LCD's, LED's, and OLED's, as used in automobiles, computers, mobile phone handsets, and televisions may also incorporate connections made by the methods described herein. Other electronic components that may similarly incorporate such technology include, but are not limited to: ASIC chips, memory devices, MCU, high frequency device modules, integrated passive components, etc.

[0038] The methods described herein can also be used to create interconnects, thermal vias or heat conductors or non-heat conductors, inductors, capacitors and resistors, to the extent that they benefit from techniques that create connections between two layers of materials. The method can further be used for optoelectronic devices such as photonic crystals, wave guides, filters, optoelectronic circuits, etc. The method can also be used for biological devices, or mixed biological and silicon-based devices, such as lab-on-a-chip arrays, and probes for bio-diagnostics.

Structure

[0039] The apparatus created by the process described herein comprises a carrier with nanostructures embedded within the carrier, wherein the nanostructures were grown to have a specific morphology and functionality. The nanostructures are oriented so as to be approximately parallel to each other and perpendicular to the substrate. The nanostructures are of an approximate desired length or height.

[0040] FIGs. 1 - 8 illustrate, schematically, the methods and apparatus described herein. It would be understood that, although FIG.s 1 - 8 have been illustrated using a carbon nanofiber (CNF), other forms of nanostructures may similarly be used. Such alternative nanostructures include, but are not limited to, nanotubes, nanowires, and nanoropes. Such nanostructures may be made from carbon, doped with one or more other elements, but are not

so limited.

[0041] FIG. 1 illustrates the overall principle of bonding and electrical contacting of two adjacent metal layers, such as a die to a substrate, using a pad of carbon nanofibers in a matrix. Shown in FIG. 1 are three layers: a substrate 100 having an embedded contact pad 110, on top of which is a layer of adhesive polymer 200 that surrounds a number of carbon nanofibers (CNF) 210 oriented perpendicularly to the substrate 100 and some of which are in contact with contact pad 110, and on top of the adhesive polymer layer is a device layer 300. The device layer 300 includes an I/O pad 310, to which a number of the carbon nanofibers are connected, a first metal plug 320, made from tungsten as an example, on top of the I/O pad, and a second metal plug 330, on top of the first plug. Plugs 320, 330 are different from one another, and can be made of tungsten or any other metal used in the industry such as Al, Cu, or Au.

[0042] FIG. 2 shows bonding and electrical contacting of a die to a substrate using carbon nanofibers in a matrix, prior to curing. Only a single CNF is shown in this figure, purely for ease of illustration.

[0043] FIGs. 3A, 3B show bonding and electrical contacting of a die to a substrate using carbon nanofibers (only a single CNF is shown in FIG. 3A, for ease of depiction) in an adhesive polymer matrix, after curing. Double-headed arrow 220 indicates a straightening force inducing a "spring load" in the CNF. Two single headed arrows 230 indicate a contracting adhesive force induced by curing.

[0044] FIG. 3B shows bonding and electrical contacting of a die to a substrate using carbon nanofibers in a matrix, after curing. Double-headed arrow 220 indicates a straightening force inducing "spring load" in the CNF. Two single headed arrows 230 indicate a contracting adhesive force induced by curing.

[0045] FIG. 4 shows a view from the top of an array of carbon nanofibers in a matrix. Representative spacings are shown. The pitch between adjacent nanostructures is 200 nm; the dimension of the array is 600 nm; and the nanofibers have a diameter of 50 nm.

[0046] FIG. 5 shows a view from the top of an array of carbon nanofibers in a matrix with an I/O pad overlaying a subset of the nanostructures. Representative spacings are shown. The pitch between adjacent nanostructures is 200 nm; the dimension of the array is 600 nm; and the nanofibers have a diameter of 50 nm; the diameter of the I/O pad is shown as 400 nm.

[0047] It would be understood by one skilled in the art that the spacings shown in FIGs. 4 and 5 are exemplary, and that the operation of technology herein is not dependent on the precise values of those spacings, as shown in the figures.

[0048] FIG. 6 shows a cross-sectional view of carbon nanofibers in a matrix with an I/O pad, such as that shown in FIG. 5. Certain of the nanostructures connect the contact pad and the I/O pad, whereas others are disposed outside of the area that the pads have in common and

need not, as shown, extend through the entire thickness of the adhesive layer.

Example 1: Process for Creating Contacts Using Nanostructures and an ACF

[0049] This example provides a method of connecting two surfaces/layers (such as between a contact surface/layer of a first die or chip, and a contact layer/surface of a second die or chip to which the first is going to be attached). The connection is by bonding and electrically/thermally contacting with any pitch in the range of 1 millimetre to 2 nm and typically down to 20 nm where the electrically/thermally contacting elements are based on nanostructures.

[0050] A structure consistent with this method consists of: (a) a layer of carrier (such as based on flexible, or solid material, for example polyimide), (b) nanostructures embedded in the carrier with specific morphology and functionality where they are oriented parallel with each other and perpendicular to both carrier surfaces, and (c) where the nanostructures can be grown according to methods described in international patent application PCT/SE2006/000487 (which is hereby incorporated by reference) such that control is demonstrated over morphology, dimension, length, distance, etc.

[0051] A typical nanostructure assembly for use herein comprises: a conducting substrate (such as a metal); a first catalyst layer on the conducting substrate; a nanostructure supported by the first catalyst layer; and a plurality of intermediate layers between the conducting substrate and the first catalyst layer, the plurality of intermediate layers including at least one layer that affects a morphology of the nanostructure and at least one layer to affect an electrical property of an interface between the conducting substrate and the nanostructure.

[0052] Features of the structure include: the contacting elements (nanostructures) are perpendicular to the connecting surfaces, although the nanostructures are parallel with each other. The properties of the nanostructures can be tailored according to methods of growth. Each unit can be combined with other such units for assembly into further structures, much as building blocks, like Lego, can be.

[0053] FIG. 7 illustrates steps in an exemplary process for connecting two surfaces or layers by bonding and creating electrical or thermal contacts comprising nanostructures. The steps comprise: growing a layer of carbon nanostructures on a conducting substrate with a plurality of intermediate layers between the conducting substrate and the nanostructures (701); spincoating the resulting nanostructures with an adhesive polymer to form a film with embedded nanostructures (702); polishing the film to create nanostructures of a uniform desired length (703); dicing the film to create individual pads (704); lifting the pads (705); applying each pad between a first conductive surface or layer (e.g., the surface of a die) and a second conductive surface or layer (of, for example, a

contact on a chip) (706); and curing the pads, such that the die is bonded to the pad and the pad is bonded to the contacting surface, thus creating electrical or thermal contacts between the die and the contacting surface by way of the nanostructures embedded within the pad (707).

[0054] The first step (701) of growing the layer of nanostructures on a conducting substrate with a plurality of intermediate layers between the conducting substrate and the nanostructures comprises growing the nanostructures, typically with a density of greater than 10 nanostructures per μm . Such a density, or the required density in a given instance, may be achieved by controlled application of catalyst dots on the substrate. Nanostructures are preferably grown using any of the various CVD-based methods, but may be grown or formed using any standard technique.

[0055] The second step (702) of spincoating the resulting nanostructures with an adhesive polymer to form a film with embedded nanostructures may be accomplished using any standard spincoating or equivalent technique of forming a carrier for the nanostructures (in a film or other layer), wherein the nanostructures are embedded within the carrier. Such a carrier may comprise an adhesive polymer or any other equivalent material that is able to adhere to a die and a contacting surface, by way of curing, pressure, heat, or other equivalent processes. The methods described herein are not limited to the exemplary embodiment of spincoating or the exemplary embodiment of use of an adhesive polymer that may be cured.

[0056] The third step (703) of polishing the carrier to achieve a uniform desired length for the nanostructures may be accomplished using any standard technique of polishing appropriate to the instant technology, whether mechanical, chemical, or otherwise. The determination of whether the nanostructures have attained the uniform desired length may, likewise, be made using any standard technique known or utilized within the art or related arts. This step is optional.

[0057] The fourth step (704) of dicing the carrier to create individual pads may be accomplished using any standard technique of dicing or otherwise creating individual pads of a desired shape and size.

[0058] The fifth step (705) of lifting the individual pads (portions of film comprised of vertically aligned carbon nanostructures embedded in adhesive polymer) may be accomplished using any standard technique of lifting such pads.

[0059] The sixth step (706) of applying each pad between a first conductive surface (of, for example, a die) and a second conductive surface (of, for example, a contact on a chip) may be accomplished using any standard technique of applying and positioning such a pad in such a location.

[0060] The seventh step (707) of curing the pads results in creation of a bond, wherein the pad is sandwiched between, and bonded to, both conductive surfaces. This

bond creates electrical or thermal contacts between the two conductive surfaces by way of the nanostructures embedded within the pad. This step is not limited to curing an adhesive polymer; it may comprise any standard technique of causing adhesion between the nanostructures embedded within the pad and the die on one side of the pad and the contacting surface on another side of the pad.

[0061] This overall process has several advantages: eliminating the need for traditional bumps, reducing the minimum possible distance between the two conductive surfaces, decreasing both the height and width of the contact points, allowing for an increase in the number and density of the contact points, eliminating complications related to the need to control the degree of pressure applied to the ACF, and enabling finer pitches by replacing particles with nanostructures, and reducing the risk of misalignment.

[0062] Consistent with the instant example, a controllable density of nanostructures (NS) per micrometer permits an increase in the effective contact points, when compared to current solutions based on spherical particles. For example, 100 NS/micrometer square (with an NS diameter of 50 nm) gives 100 individual contacting points, (see also FIGs. 4 and 5). Given dimensions of the I/O point of 20 X 20 micrometer, the number of individual contacting points can be 4,000 in that region.

Example 2: Process for Creating Spring Load Connections

[0063] A carrier (which can be based on flexible, polyimide or solid material) containing vertically aligned nanostructures (NS) (parallel oriented with each other and perpendicular to both carrier surfaces, and such as prepared by steps described in Example 1) is placed between the surface of a die and a contacting surface. See FIG. 2 and FIG. 4 as examples.

[0064] By curing of the carrier containing the vertically aligned nanostructures (using heat or chemical components or light), the carrier will contract (decreasing the distance between the die and contacting layer).

[0065] The contracting of the carrier will induce a contracting force on the vertically aligned nanostructures. The result of the contracting force on the nanostructures will be a slight bending of the nanostructures. However, due to difference in the Young modulus between the nanostructures and the surrounding materials, the nanostructures will have a tendency to straighten.

[0066] The forces described above create the "spring-load" force in the nanostructures. When the nanostructures embedded in the carrier material are placed between the two conducting surfaces, the spring-load force will secure the contacts to the ends of the nanostructures. (See FIGs. 3A and 3B as examples.)

[0067] A process of providing a spring-loaded connection by providing bonding of the die to the substrate, creating and securing the electric contact by using the NS's

embedded in carrier, is shown in FIG. 8. Steps of FIG. 8 that are common with those of FIG. 7 are described in connection with Example 1, herein, and are not repeated here.

[0068] During the sixth step (806) of curing the pads of carrier with embedded nanostructures, the curing process may use heat, or chemical components, or light to cause the carrier to contract, thereby decreasing the distance between the die and contacting layer.

[0069] The nanostructures of this example can be made according to the same methods as the nanostructures of Example 1, herein, and in particular can be grown according to methods described in international patent application PCT/SE2006/000487 such that control is demonstrated over morphology, dimension, length, distance, etc.

[0070] The process described in this example can be utilized to address the lead breakage and misalignment issues that can arise with Chip On Flex applications.

[0071] Similarly to the structures of Example 1, properties of the spring-loaded structure include: the contacting elements (nanostructures) are perpendicular to the connecting surfaces, although the nanostructures are parallel with each other. The properties of the nanostructures can be tailored according to methods of growth. Each unit can be combined with other such units for assembly into further structures.

[0072] This overall process has several advantages: reducing the minimum possible distance between the two conductive surfaces, decreasing both the height and width of the contact points, allowing for an increase in the number and density of the contact points thereby increasing the effective contact area, eliminating complications related to the need to control the degree of pressure applied to the ACF, enabling finer pitches by replacing particles with nanostructures, and reducing the risk of misalignment, and securing of the electric contact between two points placed on the opposite surfaces using nanostructures which are slightly bent. When the nanostructures are slightly bent it is possible to minimize gap creation due to surface roughness in the bonding surfaces.

[0073] Consistent with the instant example, a controllable density of nanostructures (NS) per micrometer permits an increase in the effective contact points, when compared to current solutions based on spherical particles. For example, a controllable nanostructure diameter ranging from 1 nm to 200 nm) gives a predefined individual contact point and a contact area per nanometers square.

Example 3: Wafer level bumping (WLB)

[0074] This example demonstrates how wafer level bumping can be achieved by growing a matrix of nanostructures on I/O points on electronic circuits to thereby create electronic assembly for dies. The method can also be a method of connecting two surfaces/layers (contact

surface/layer of the die or chip, and contact layer/surface of the die or chip to which the first layer will be connected), by bonding and electrically and/or thermally contacting with any pitch in range of 1 centimeter to 2 nm, and typically down to 1 μm , where the electrically/thermally contacting elements are based on nanostructures.

[0075] The following three cases illustrate possible embodiments.

10 Case 1: Vertically aligned nanostructures grown on I/O points on a integrated circuits of a wafer thereby creating a matrix structures and embedded in a curable (in UV/laser/light) material with adhesive nature, which is corresponding to the connecting points on a substrate where the die needs to be connected to.

15 Case 2: Vertically aligned nanostructures grown on I/O points on a integrated circuits of a wafer thereby creating a matrix structures and which is corresponding to the connection points on a substrate at which the die needs to be connected, and the attachment is made via traditional high temperature soldering process.

20 Case 3: Vertically aligned nanostructures grown on I/O points on an integrated circuit of a wafer creating a matrix structure, which is corresponding to the connecting points on a substrate at which the die needs to be connected.

25 **[0076]** In general, similarly to the structures of Examples 2 and 3, properties of the wafer level bumping structure include: the contacting elements (nanostructures) are perpendicular to the connecting surfaces, although the nanostructures are parallel with each other. The properties of the nanostructures can be tailored according to methods of growth. The vertically aligned nanostructures can form groups of connecting structures with a dimension from 1 millimetre down to 2 nm.

30 **[0077]** The nanostructures of this example can be made according to the same methods as the nanostructures of Examples 1 and 2, herein, and in particular can be grown according to methods described in international patent application PCT/SE2006/000487 such that control is demonstrated over morphology, dimension, length, distance, etc.

35 **[0078]** A process of providing a wafer-level bump is shown in FIG. 9. Steps of FIG. 9 that are common with those of FIGs. 7 and 8 are described in connection with Examples 1 and 2, herein, and are those descriptions are not repeated here.

40 **[0079]** In current systems, bumps for can have a diameter from 500 micrometer and downwards. The method of this example permits a groups of nanostructures to be assembled, each individual group having the same dimension as today's bumps. However, the present technique also permits smaller bumps, even down to bumps

that comprise a single nanostructure.

[0080] Composite bumps can also be formed by methods based on those described herein. Standard evaporation, electroplating and/or electroless plating can be carried out after the growth of nanostructures to form composite bumps where necessary. Different metals/metallic materials from periodic table such as Ti, Cr, TiW, Cu, Au or any other suitable metal can be evaporated, electroplated, and /or electroless plated after the growth of nanostructures. Standard immersion gold process can also be carried out to coat gold where necessary. Electroless plating process may consist of conditioning, acid etching, plating through different chemical compositions for different metal for example, Ni, Cu, Zn, Sn, or different alloys.

Claims

1. A bonding film, for interconnecting a first conductive surface (110) with a second conductive surface (310) through said bonding film, wherein said bonding film comprises a plurality of nanostructures (210) embedded in a polymeric carrier (200), said nanostructures (210) being oriented in parallel with each other and extending perpendicularly to top and bottom surfaces of said polymeric carrier (200), wherein said polymeric carrier (200) is configured to:
 - adhere to said first conductive surface (110) and said second conductive surface (310) when arranged there between with the nanostructures being oriented perpendicular to said first and second conductive surfaces; and
 - contract when cured.
 2. The bonding film according to claim 1, wherein said nanostructures (210) are electrically or thermally conductive.
 3. The bonding film according to claim 2, wherein each of said nanostructures (210) comprises two or more interdiffused materials, the two or more interdiffused materials including at least one material that affects a morphology of said plurality of nanostructures and at least one material that affects an electrical property of an interface between said first and second conductive surfaces and said plurality of nanostructures.
 4. The bonding film according to claim 3, wherein at least one material of the two or more interdiffused materials is present at a tip of each of said nanostructures (210).
 5. The bonding film according to claim 3 or 4, wherein at least one material of the two or more interdiffused
6. An electronic device comprising:
 - an electronic component having a first conductive surface (310);
 - a substrate (100) having a second conductive surface (110); and
 - the bonding film according to any one of claims 1 to 5 being arranged between said conductive surface of the electronic component (310) and said conductive surface of the substrate (110), wherein the polymeric carrier (200) comprised in said bonding film is in a cured state and the nanostructures (210) comprised in said bonding film are pressed against said conductive component surface (310) and said conductive substrate surface (110) through a spring-load force.
 7. A method of forming the bonding film according to any one of claims 1 - 5, comprising the steps of:
 - growing (701) a plurality of nanostructures on a conductive substrate in such a way that said nanostructures extend perpendicularly to said conductive substrate;
 - coating (702) said nanostructures with a carrier to form said bonding film on said conductive substrate; and
 - lifting (705) said bonding film from said conductive substrate, wherein said carrier is a polymeric carrier configured to contract when cured.
 8. The method according to claim 7, further comprising the step of:
 - polishing (703) said bonding film to provide a uniform length of said nanostructures.
 9. The method according to claim 7 or 8, further comprising the step of:
 - dicing (704) said carrier into individual films.
 10. The method according to any one of claims 7 to 9, wherein said carrier is an adhesive polymer.
 11. The method according to any one of claims 7 to 10, wherein said step of growing comprises the steps of:
 - depositing one or more intermediate layers on the conductive substrate;
 - depositing a catalyst layer on the one or more intermediate layers;
 - without first annealing the substrate, causing the substrate to be heated to a temperature at which the nanostructures can form; and
 - growing two or more nanostructures on the cat-

alyst layer at the temperature, wherein at least one of the one or more intermediate layers are interdiffused with the catalyst layer, and wherein the catalyst layer and the at least one of the one or more intermediate layers that are interdiffused are present in the nanostructure.

12. The method according to claim 11, further comprising the step of:
coating the nanostructures with metal deposition to form metal embedded nanostructures on said conductive substrate.

Patentansprüche

1. Bonding-Film zum Verbinden einer ersten leitfähigen Fläche (110) mit einer zweiten leitfähigen Fläche (310) durch den Bonding-Film, wobei der Bonding-Film mehrere Nanostrukturen (210) umfasst, die in einen Polymerträger (200) eingebettet sind, wobei die Nanostrukturen (210) parallel zueinander orientiert sind und sich senkrecht zu einer oberen und unteren Fläche des Polymerträgers (200) erstrecken, wobei der Polymerträger (200) konfiguriert ist zum:

Kleben an der ersten leitfähigen Fläche (110) und der zweiten leitfähigen Fläche (310), wenn er dazwischen angeordnet wird, wobei die Nanostrukturen senkrecht zu der ersten und zweiten leitfähigen Fläche orientiert sind; und Zusammenziehen, wenn er gehärtet wird.
2. Bonding-Film nach Anspruch 1, wobei die Nanostrukturen (210) elektrisch oder thermisch leitfähig sind.
3. Bonding-Film nach Anspruch 2, wobei jede der Nanostrukturen (210) zwei oder mehr interdiffundierte Materialien umfasst, wobei die zwei oder mehr interdiffundierten Materialien mindestens ein Material, welches eine Morphologie der mehreren Nanostrukturen beeinflusst, und mindestens ein Material umfasst, welches eine elektrische Eigenschaft einer Grenzfläche zwischen der ersten und der zweiten leitfähigen Fläche und den mehreren Nanostrukturen beeinflusst.
4. Bonding-Film nach Anspruch 3, wobei mindestens ein Material der zwei oder mehr interdiffundierten Materialien an einer Spitze jeder der Nanostrukturen (210) vorhanden ist.
5. Bonding-Film nach Anspruch 3 oder 4, wobei mindestens ein Material der zwei oder mehr interdiffundierten Materialien aus der Gruppe ausgewählt ist,

die aus amorphem Silizium und Germanium besteht.

6. Elektronische Vorrichtung, umfassend:

5 eine elektronische Komponente mit einer ersten leitfähigen Fläche (310);
ein Substrat (100) mit einer zweiten leitfähigen Fläche (110); und
den Bonding-Film nach einem der Ansprüche 1 bis 5, angeordnet zwischen der leitfähigen Fläche der elektronischen Komponente (310) und der leitfähigen Fläche des Substrats (110), wobei der in dem Bonding-Film enthaltene Polymerträger (200) in einem gehärteten Zustand vorliegt und die in dem Bonding-Film enthaltenen Nanostrukturen (210) durch eine Federkraft gegen die leitfähige Komponentenfläche (310) und die leitfähige Substratfläche (110) gedrückt werden.

7. Verfahren zum Bilden des Bonding-Films nach einem der Ansprüche 1 bis 5, umfassend die Schritte:

20 Anwachsenlassen (701) mehrerer Nanostrukturen auf einem leitfähigen Substrat auf solche Weise, dass sich die Nanostrukturen senkrecht zu dem leitfähigen Substrat erstrecken;
Beschichten (702) der Nanostrukturen mit einem Träger zum Bilden des Bonding-Films auf dem leitfähigen Substrat; und
Abheben (705) des Bonding-Films von dem leitfähigen Substrat, wobei der Träger ein Polymerträger ist, der dafür konfiguriert ist, sich zusammenzuziehen, wenn er gehärtet wird.

8. Verfahren nach Anspruch 7, ferner umfassend den Schritt:

40 Polieren (703) des Bonding-Films, um für eine einheitliche Länge der Nanostrukturen zu sorgen.

9. Verfahren nach Anspruch 7 oder 8, ferner umfassend den Schritt:

45 Schneiden (704) des Trägers zu einzelnen Filmen.

10. Verfahren nach einem der Ansprüche 7 bis 9, wobei der Träger ein klebendes Polymer ist.

11. Verfahren nach einem der Ansprüche 7 bis 10, wobei der Schritt des Anwachsenlassens die Schritte umfasst:

50 Abscheiden einer oder mehrerer Zwischenschichten auf dem leitfähigen Substrat;
Abscheiden einer Katalysatorschicht auf der einen oder den mehreren Zwischenschichten;
Bewirken, dass das Substrat auf eine Temperatur erwärmt wird, bei welcher sich die Nanos-

strukturen bilden können, ohne das Substrat zunächst zu tempern; und

Anwachsenlassen von zwei oder mehr Nanostrukturen auf der Katalysatorschicht bei der Temperatur, wobei mindestens eine der einen oder der mehreren Zwischenschichten mit der Katalysatorschicht interdiffundiert und wobei die Katalysatorschicht und mindestens eine der einen oder der mehreren Zwischenschichten, die interdiffundiert sind, in der Nanostruktur vorliegt.

12. Verfahren nach Anspruch 11, ferner umfassend den Schritt:

Beschichten der Nanostrukturen durch Metallabscheidung zum Bilden von eingebetteten Metall-Nanostrukturen auf dem leitfähigen Substrat.

Revendications

- 1.** Film de liaison, permettant d'interconnecter une première surface conductrice (110) avec une seconde surface conductrice (310) grâce audit film de liaison, dans lequel ledit film de liaison comprend une pluralité de nanostructures (210) incorporées dans un support polymère (200), lesdites nanostructures (210) étant orientées en parallèle l'une par rapport à l'autre et s'étendant de manière perpendiculaire à des surfaces supérieures et inférieures dudit support polymère (200), dans lequel ledit support polymère (200) est conçu pour :

adhérer à ladite première surface conductrice (110) et à ladite seconde surface conductrice (310) lorsqu'il est agencé entre celles-ci avec les nanostructures étant orientées perpendiculairement audit première et seconde surfaces conductrices ; et se contracter lors du durcissement.

- 2.** Film de liaison selon la revendication 1, dans lequel lesdites nanostructures (210) sont électriquement ou thermiquement conductrices.
- 3.** Film de liaison selon la revendication 2, dans lequel chacune desdites nanostructures (210) comprend deux ou plusieurs matériaux inter-diffus, les deux ou plusieurs matériaux inter-diffus comprenant au moins un matériau qui a un effet sur la morphologie de ladite pluralité de nanostructures et au moins un matériau qui a un effet sur une propriété électrique d'une interface entre lesdites première et seconde surfaces conductrices et ladite pluralité de nanostructures.
- 4.** Film de liaison selon la revendication 3, dans lequel au moins un matériau parmi les deux ou plusieurs

matériaux inter-diffus est présent au niveau d'une pointe de chacune desdites nanostructures (210).

- 5.** Film de liaison selon la revendication 3 ou la revendication 4, dans lequel au moins un matériau parmi les deux ou plusieurs matériaux inter-diffus est choisi dans le groupe constitué du silicium et du germanium amorphe.

- 6.** Dispositif électronique comprenant :

un composant électrique ayant une première surface conductrice (310) ;

un substrat (100) ayant une seconde surface conductrice (110) ; et

le film de liaison selon l'une quelconque des revendications 1 à 5 étant agencé entre ladite surface conductrice du composant électronique (310) et ladite surface conductrice du substrat (110),

dans lequel le support polymère (200) compris dans ledit film de liaison se trouve dans un état de durcissement et les nanostructures (210) comprises dans ledit film de liaison sont pressées contre ladite surface de composant conductrice (310) et ladite surface de substrat conductrice (110) grâce à une force de contrainte de ressort.

- 7.** Procédé de formation du film de liaison selon l'une quelconque des revendications 1 à 5, comprenant les étapes consistant à :

cultiver (701) une pluralité de nanostructures sur un substrat conducteur d'une manière telle que lesdites nanostructures s'étendent de manière perpendiculaire audit substrat conducteur ; revêtir (702) lesdites nanostructures avec un support afin de former ledit film de liaison sur ledit substrat conducteur ; lever (705) ledit film de liaison à partir dudit substrat conducteur, dans lequel ledit support est un support polymère conçu pour se contracter lors du durcissement.

- 8.** Procédé selon la revendication 7, comprenant en outre l'étape consistant à : polir (703) ledit film de liaison afin d'obtenir une longueur uniforme desdites nanostructures.

- 9.** Procédé selon la revendication 7 ou la revendication 8, comprenant en outre l'étape consistant à : découper en dés (704) ledit support en des films individuels.

- 10.** Procédé selon l'une quelconque des revendications 7 à 9, dans lequel ledit support est un polymère ad-

hésif.

11. Procédé selon l'une quelconque des revendications 7 à 10, dans lequel ladite étape de culture comprend les étapes consistant à :
- déposer une ou plusieurs couches intermédiaires sur ledit substrat intermédiaire ;
- déposer une couche de catalyseur sur l'une ou plusieurs couches intermédiaires ;
- sans la recuisson préalable du substrat, amener le substrat à être chauffé à une température à laquelle les nanostructures peuvent se former ;
- et
- cultiver deux ou plusieurs nanostructures sur la couche de catalyseur à la température, dans lequel au moins une de l'une ou plusieurs couches intermédiaires sont interdiffusées avec la couche de catalyseur, dans lequel la couche de catalyseur et l'au moins une de l'une ou plusieurs couches intermédiaires qui sont interdiffusées sont présentes dans la nanostructure.
12. Procédé selon la revendication 11, comprenant en outre l'étape consistant à :
- revêtir les nanostructures avec un dépôt métallique afin de former des nanostructures incorporées dans le métal sur ledit substrat conducteur.

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FIG. 1

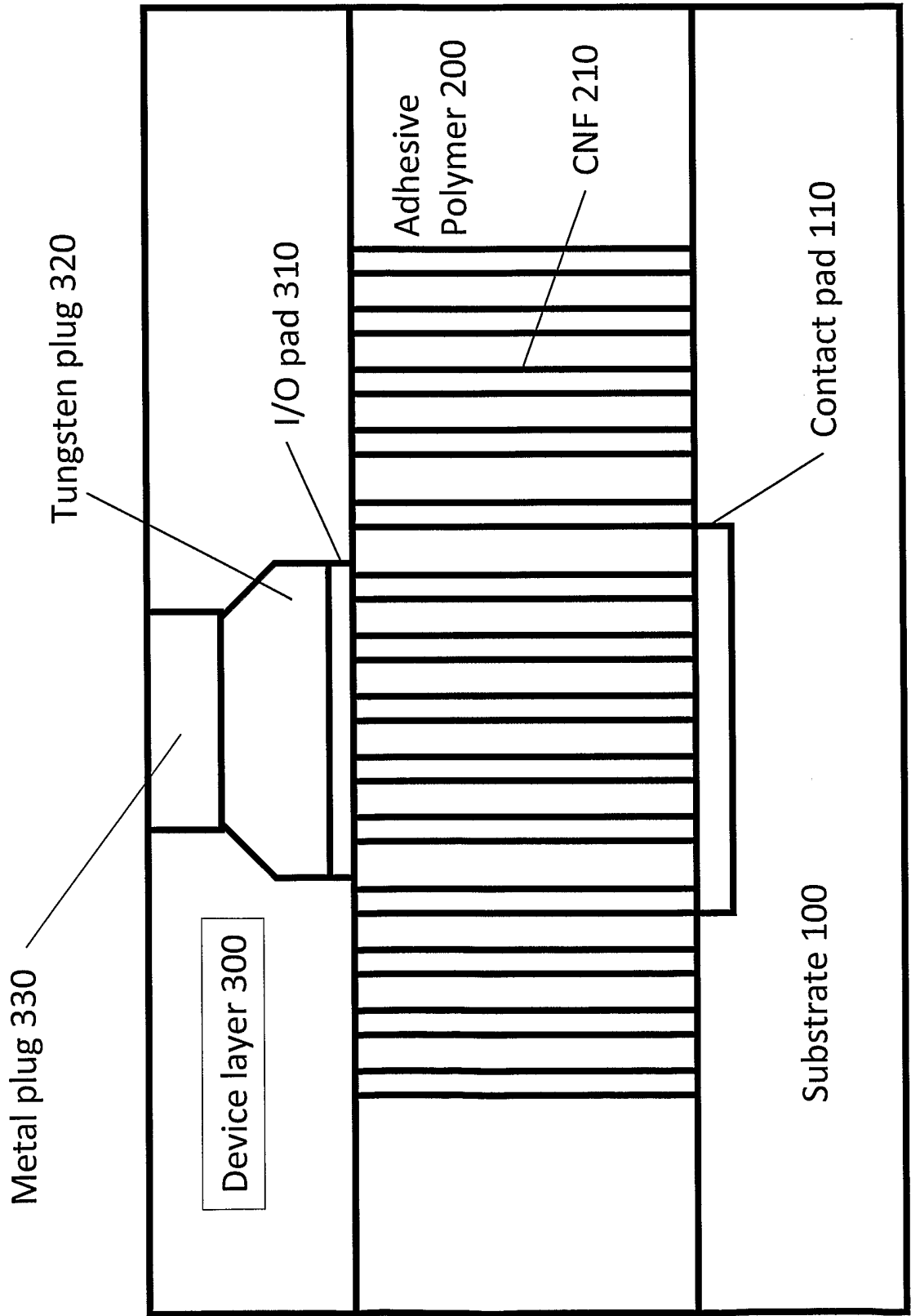
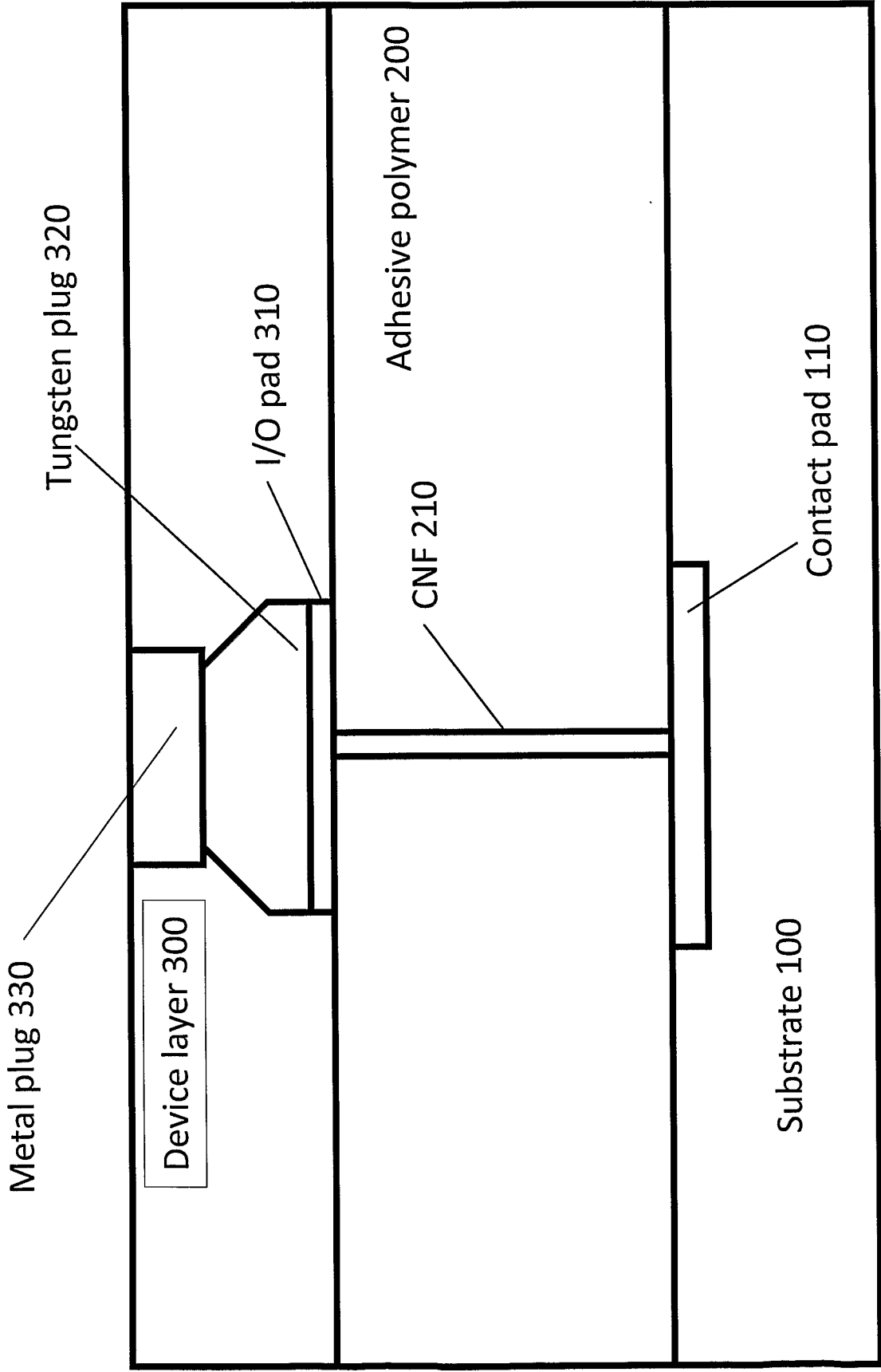


FIG. 2



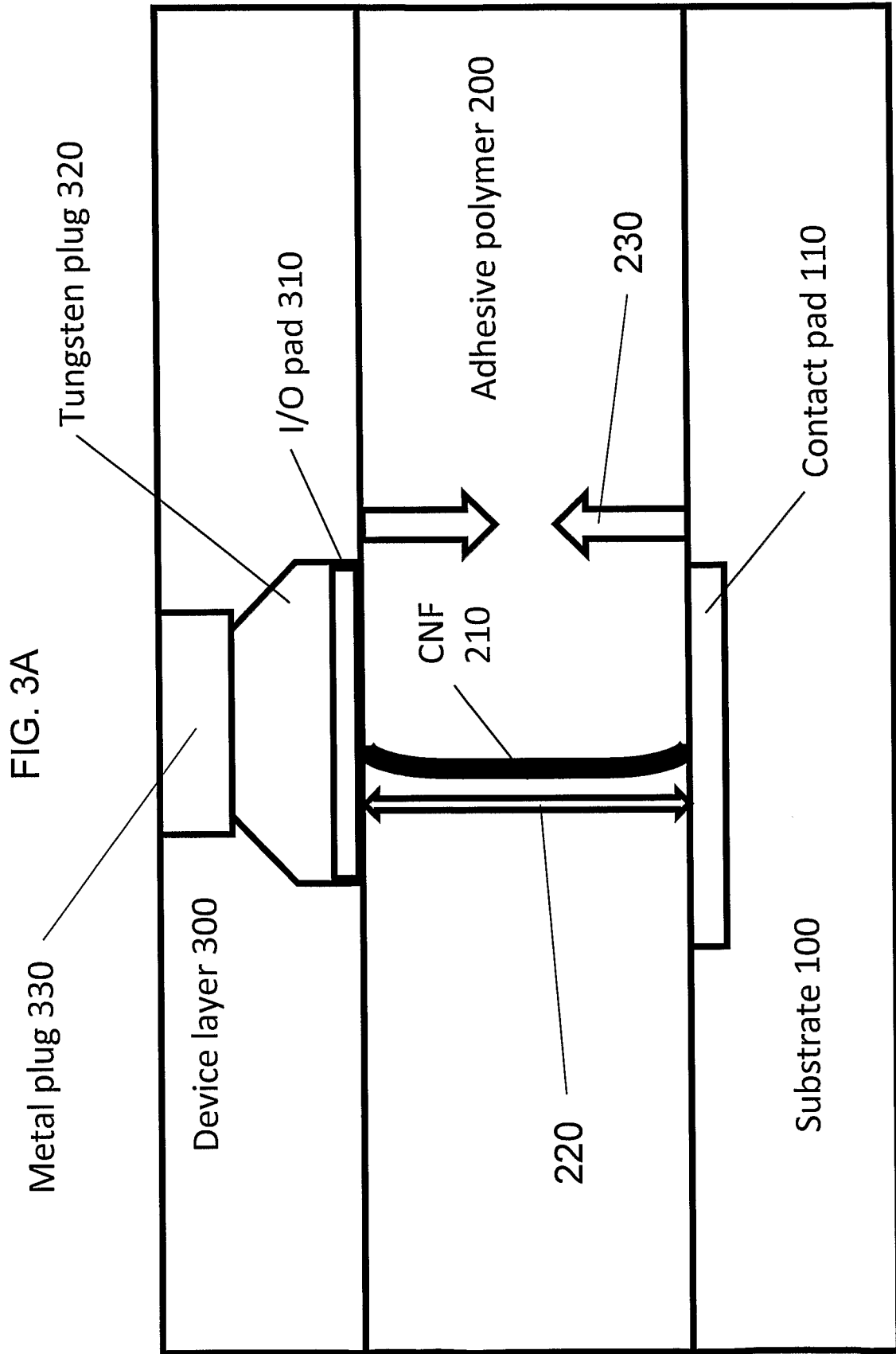


FIG. 3B

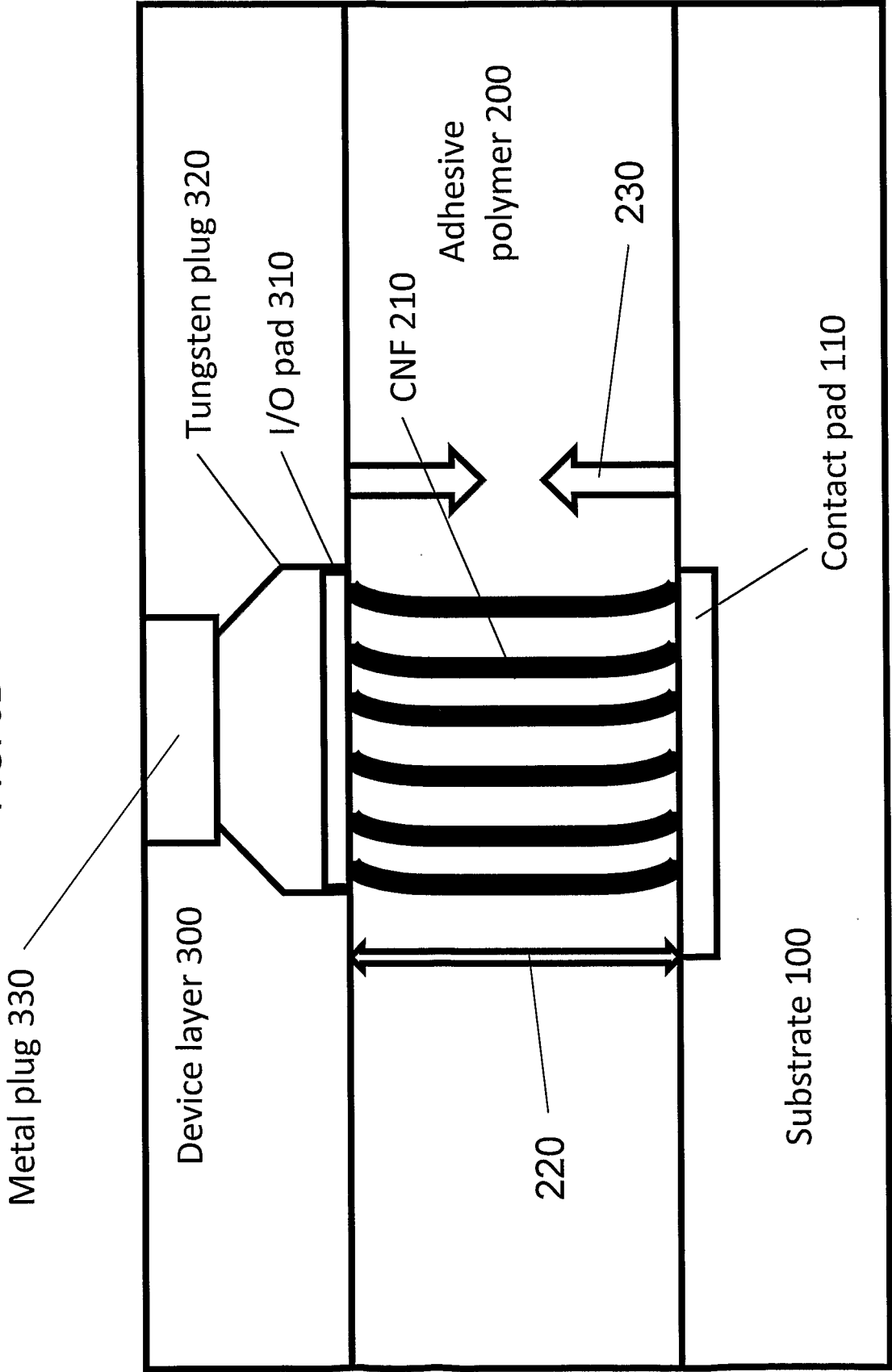


FIG. 4

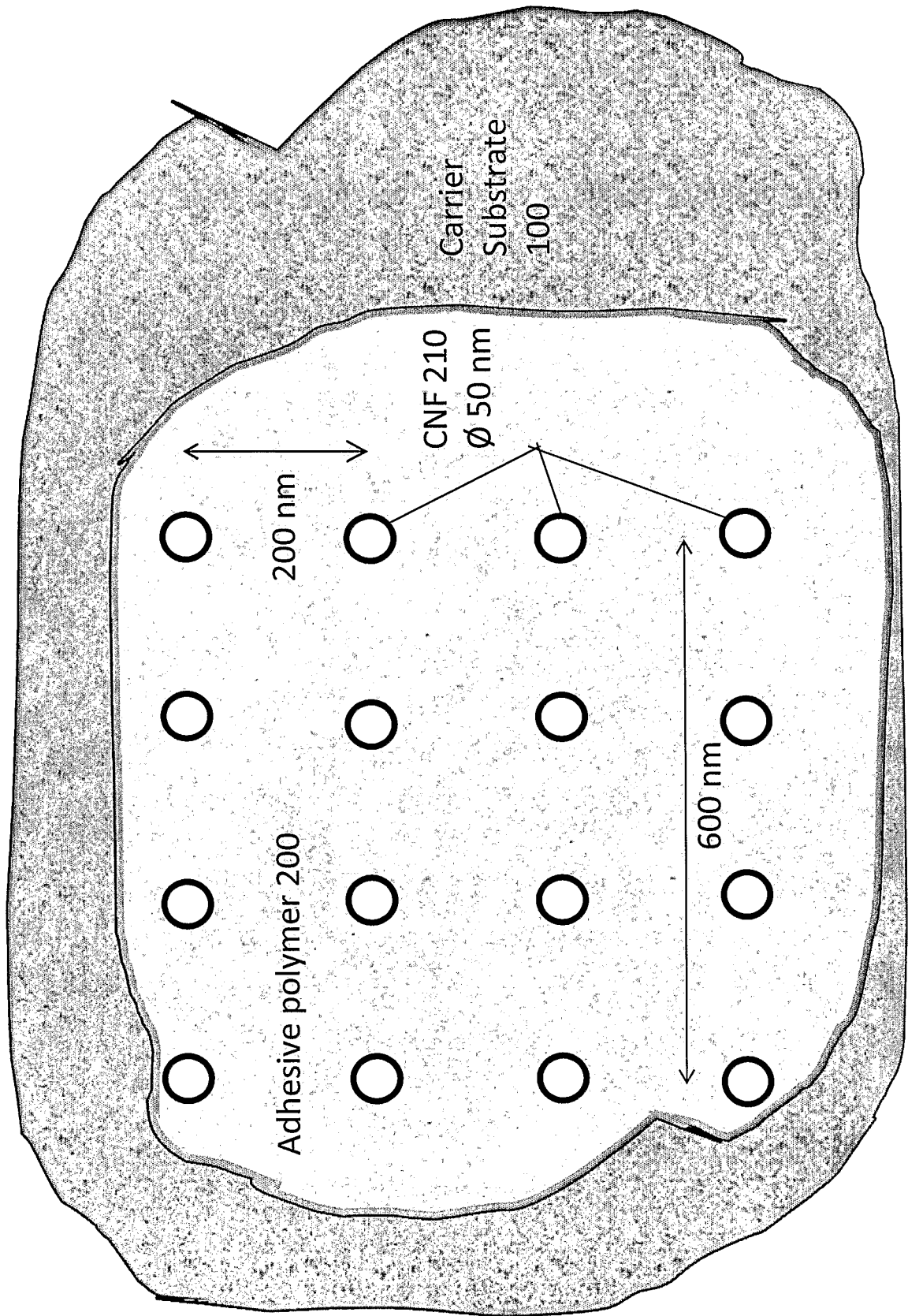


FIG. 5

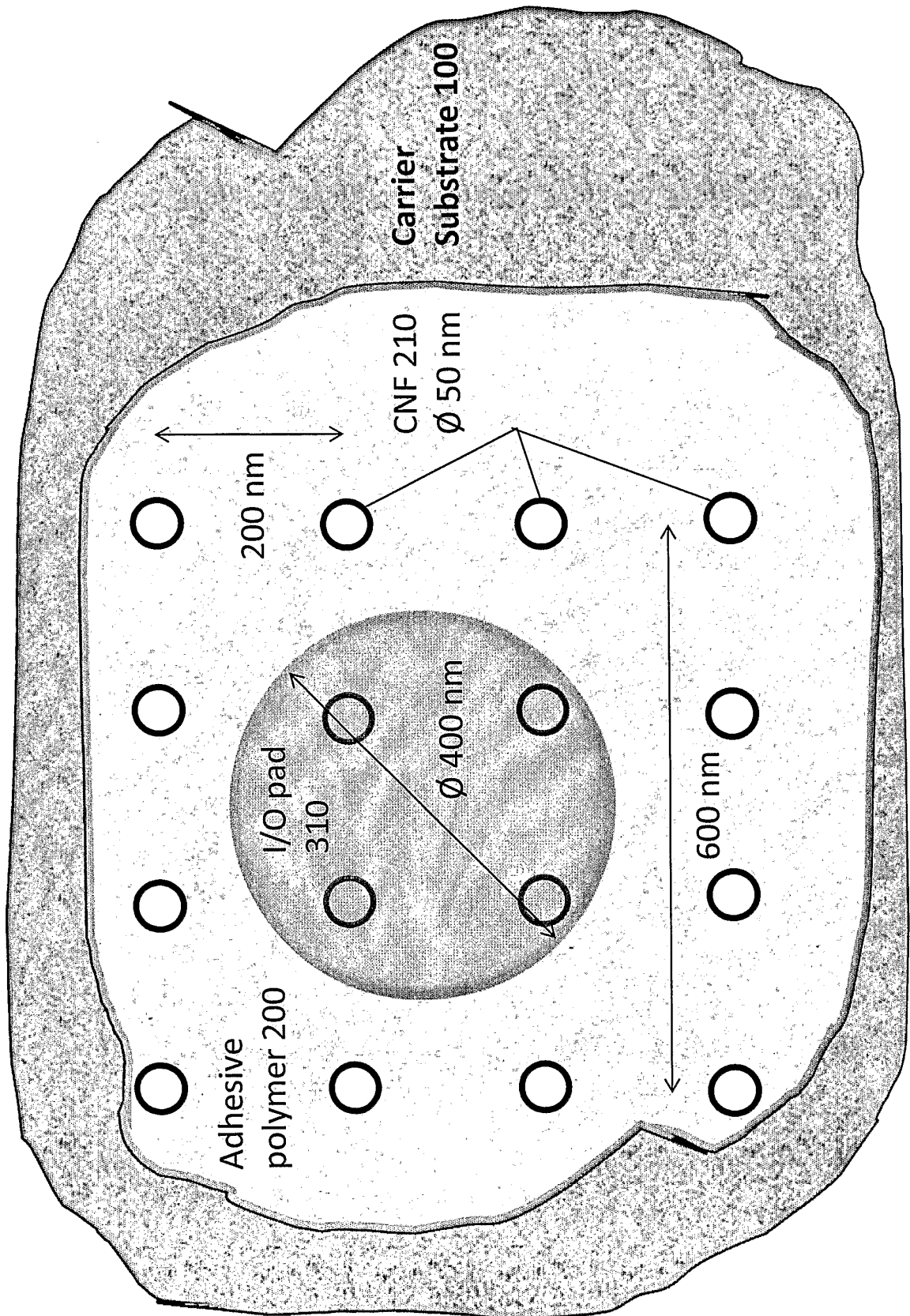
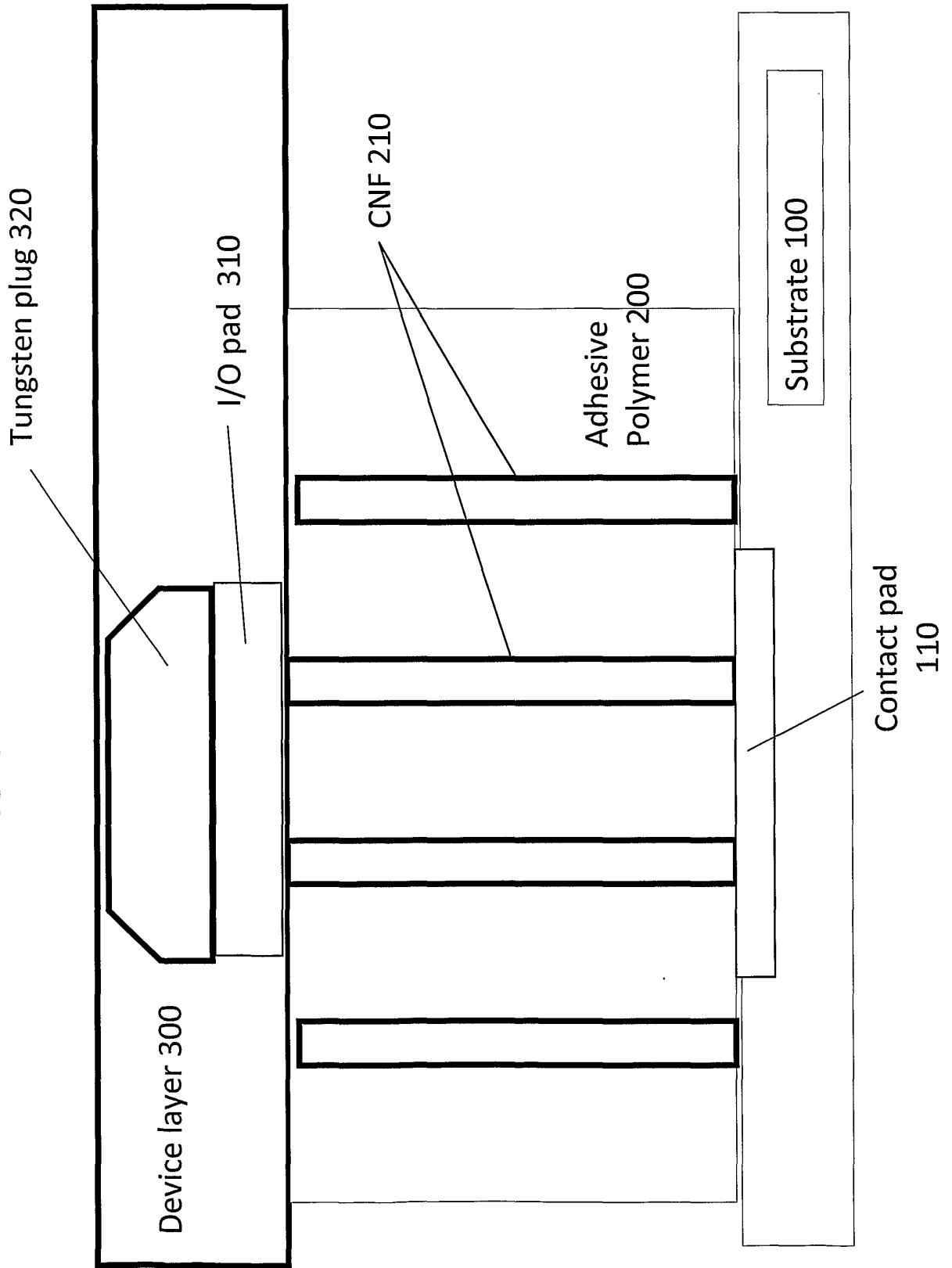


FIG. 6



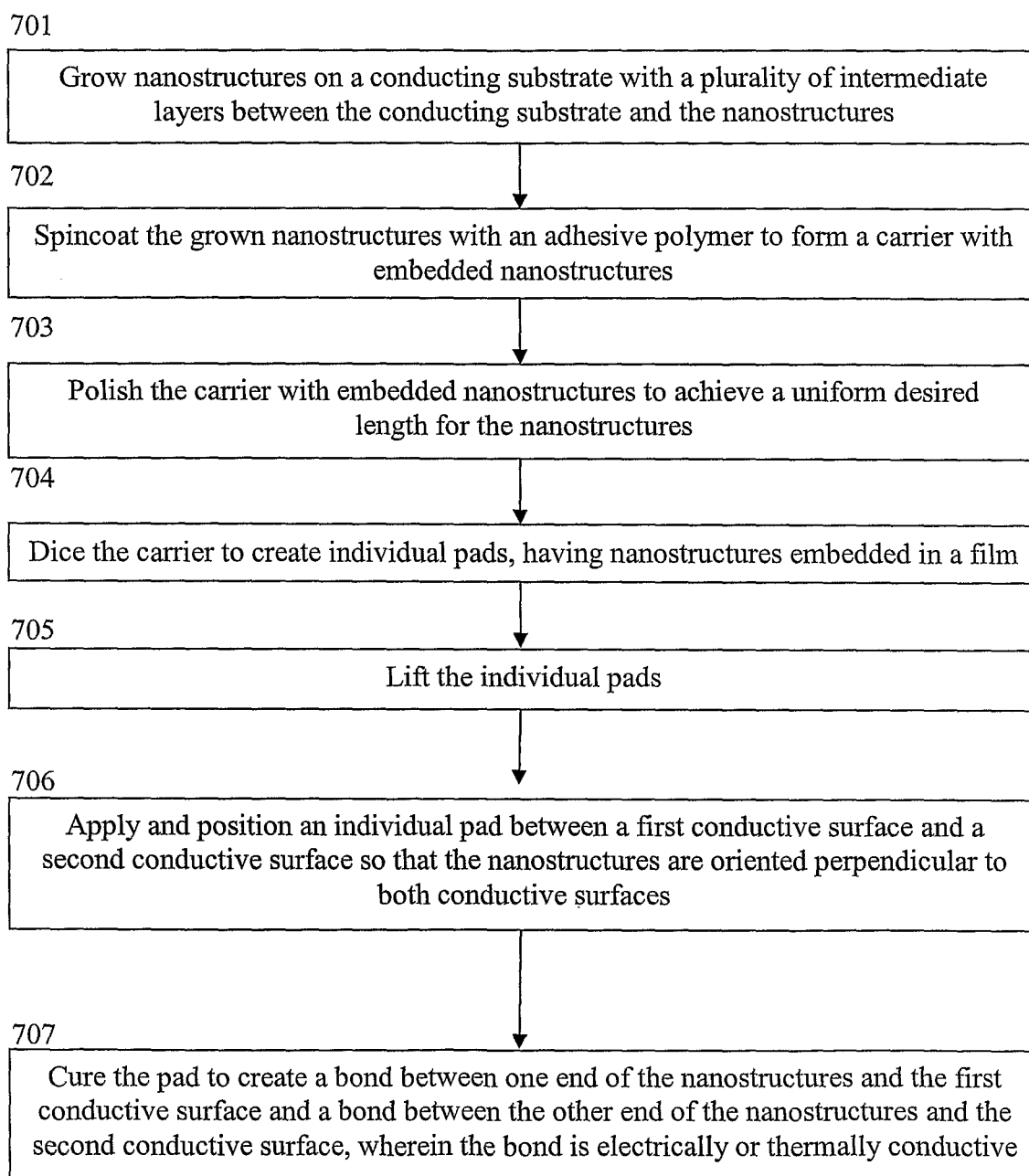


FIG. 7

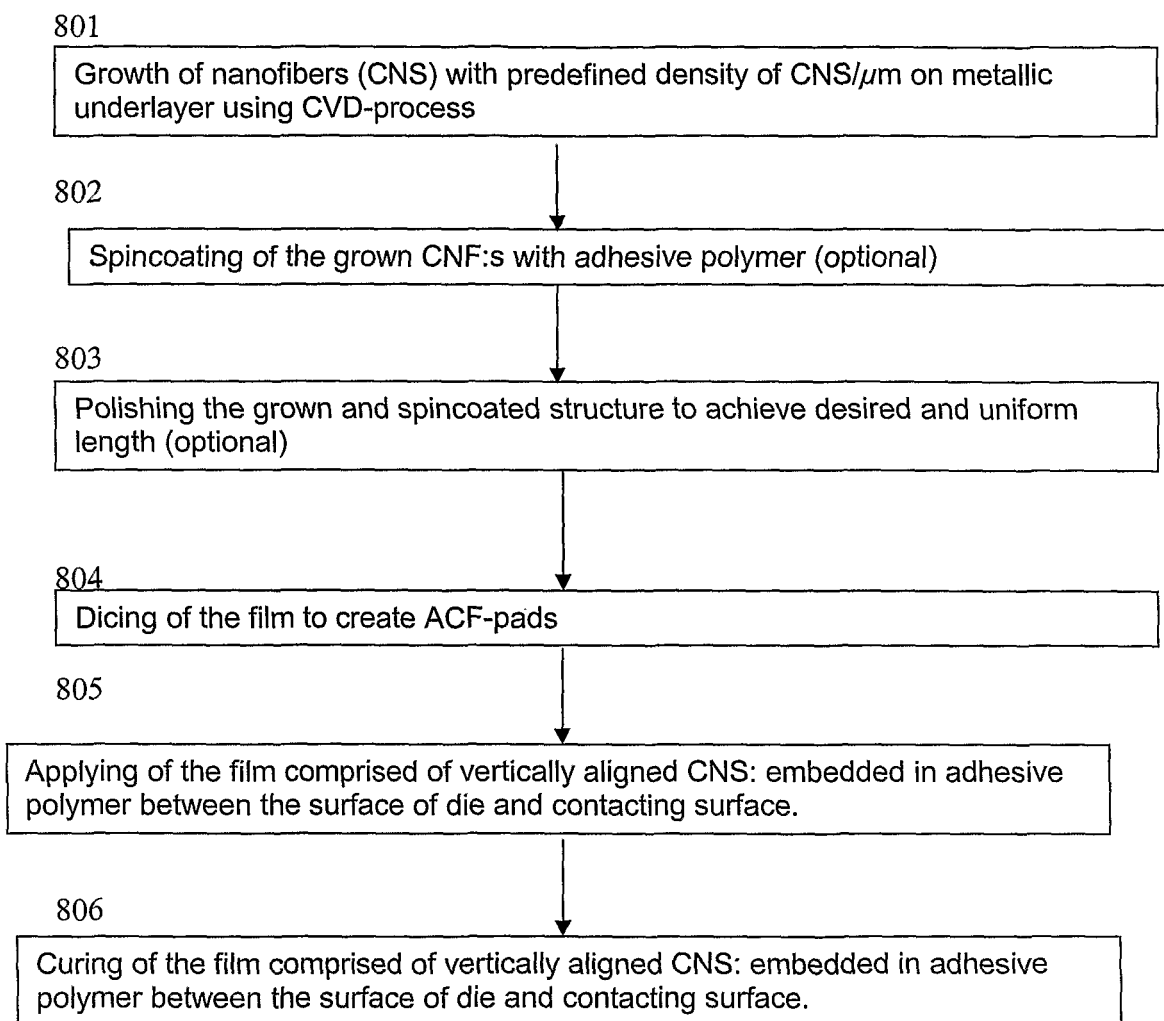


FIG. 8

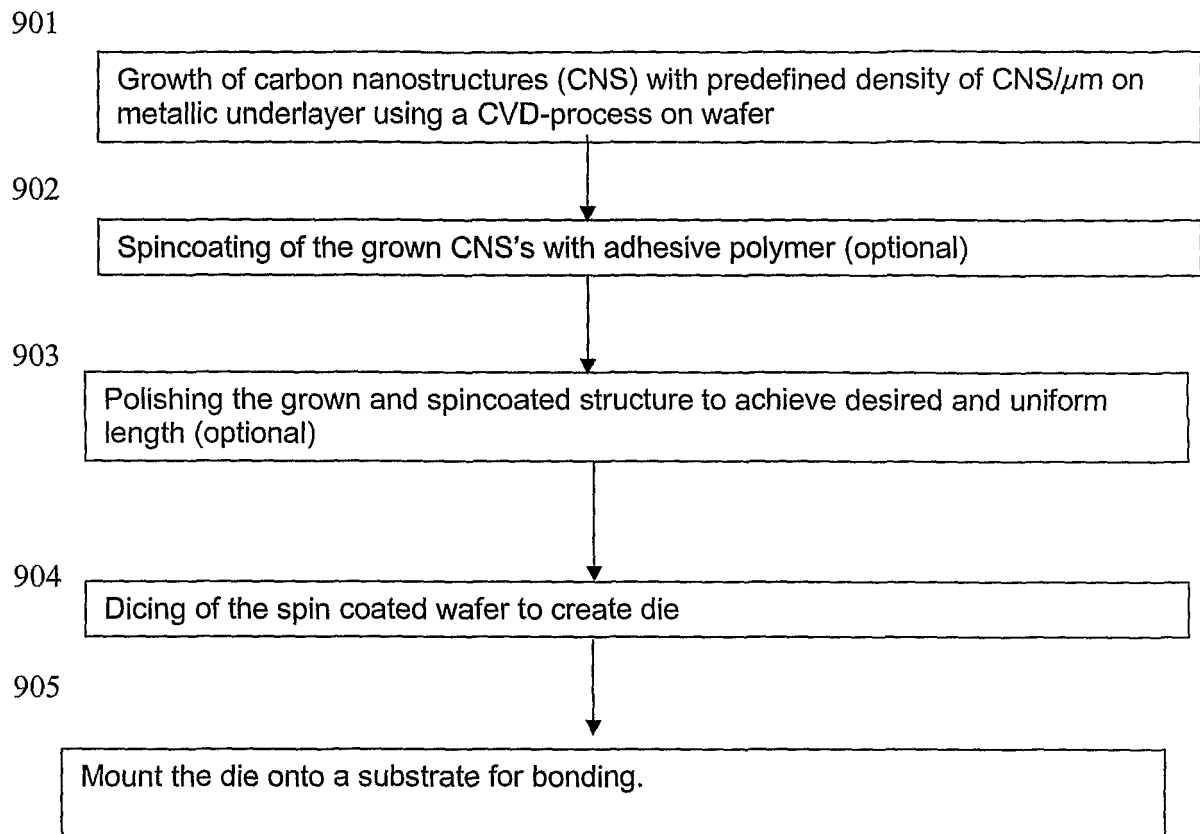


FIG. 9

REFERENCES CITED IN THE DESCRIPTION

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