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(54) DEPOSITION AND SELECTIVE REMOVAL OF CONDUCTING HELPLAYER FOR NANOSTRUCTURE PROCESSING

AUFTRAGUNG UND SELEKTIVE ENTFERNUNG EINER LEITENDEN HILFSSCHICHT FÜR NANOSTRUKTURBEARBEITUNG

DÉPÔT ET ENLÈVEMENT SÉLECTIF D'UNE COUCHE AUXILIAIRE CONDUCTRICE POUR TRAITEMENT DE NANOSTRUCTURES

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Description

TECHNICAL FIELD

[0001] The technology described herein is generally related to the field of chemical vapor deposition (CVD) of nanostructures, and more specifically to reduction or elimination of plasma-induced damages during growth of nanostructures, and enabling self-aligned growth of nanostructures on both conducting and insulating surfaces.

BACKGROUND OF THE INVENTION

[0002] The present technology described herein is related to but not limited to nanostructures such as carbon nanostructures (e.g., carbon nanotubes, carbon nanofibers, and carbon nanowires). These nanostructures have gained interest in recent years due to their high thermal and electrical conductivities.

[0003] Carbon nanostructures can be manufactured with arc discharge methods, laser ablation, or chemical vapor deposition (CVD). A catalyst is used in CVD processing to obtain growth of the nanostructures. Two most frequently used CVD methods are thermal CVD and plasma-enhanced CVD (i.e., plasma CVD). In thermal CVD, the energy required for formation of the nanostructures is thermal energy. In plasma CVD, the energy required for formation of the nanostructures is from the plasma. Plasma CVD makes it possible to grow nanostructures at a lower temperature than that used in thermal CVD. The lower growth temperature in plasma CVD is a significant advantage as the substrates on which the nanostructures grow are often damaged at excessive temperatures.

[0004] Several types of plasma CVD exist, including radio-frequency plasma CVD, inductively-coupled plasma CVD and direct-current plasma CVD. Direct-current plasma CVD (DC-CVD) is often preferred since the electric field close to the substrate surface enables alignment of the growing nanostructures. In some instances, the electric field creates nanostructure alignment that is substantially perpendicular to the substrate. In some instances, alignment with other angular deviation from the perpendicular direction can also be achieved as desired.

[0005] FIGS. 1A-1E illustrate various configurations not forming part of the invention that nanostructures can be grown on a substrate.

[0006] FIG. 1A illustrates a configuration for growing nanostructures 106 and/or 108 from a patterned catalyst layers 102 and/or 104 on a conducting substrate 100. Nanostructure 106 is a single nanostructure growing on a small catalyst dot 102, while nanostructures 108 is a "forest" of nanostructures (multiple closely-spaced nanostructures) growing on a large catalyst area 104. FIG. 1B illustrates a configuration for growing nanostructures 106 and/or 108 from a patterned catalyst layers 102 and/or 104 on a continuous metal underlayer 112 deposited on a insulating substrate 110. A small catalyst dot 102 gives rise to an individual nanostructure 106, while a large catalyst area 104 gives rise to a "forest" of nanostructures 108 (multiple closely-spaced nanostructures). These two configurations of using DC-CVD to grow nanostructures are relatively straight-forward.

[0007] However, problems arise if the patterned catalyst layers 102 and/or 104 are deposited directly on an insulator 110 (as shown in FIG. 1C) or on isolated metal islands 114 over an insulator 110 (as shown in FIG. 1D). The problems will most often occur if there are insulating areas around the metal islands, even if the metal islands are electrically connected to other parts of the substrate. Electric arcs will occur during the growth process, and cause damage to the growth structure due to sputtering. The arcs can also damage the electronic devices connected to the growth structures by the over-voltages produced by the arcs. FIG. 2 shows an example of damage caused on a substrate due to arcing. These over-voltages can damage the devices even if the devices are buried below several material layers, as the devices are electrically connected to the topmost metal layers. U.S. Patent No. 5,651,865 provides a detailed description of the problems related to having insulating regions on an otherwise conducting surface in a DC plasma.

[0008] There are some proposed solutions describing improvements of the DC power supply to reduce the problems with arcs. For example, U.S. Patent No. 5,576,939 and U.S. Patent No. 6,943,317 disclose methods for shutting down or reversing the polarity of the power supply at the onset of an arc. U.S. Patent No. 5,584,972 describes connecting an inductor and a diode between the power supply and the electrodes. U.S. Patent No. 7,026,174 discloses putting the wafer at a bias voltage in order to reduce arcing. U.S. Patent No. 5,651,865 discloses using a periodic polarity change of the plasma voltage to preferentially sputter away any insulator from an otherwise conductive surface, which does not enable the nanostructure growth on samples with insulating regions.

[0009] Methods for manufacturing nanofibers on a patterned metal underlayer have been shown for some applications in, for example, U.S. Patent No. 6,982,519. The methods disclosed consist of growing the nanofibers on a continuous metal underlayer using a patterned catalyst layer, and afterwards patterning the metal underlayer using optical lithography. The disclosed method requires a continuous metal underlayer for the growth, and the patterning of the metal underlayer is made afterwards.

[0010] This technique disclosed in U.S. Patent No. 6,982,519 is not compatible with standard (CMOS) processing of interconnect layers in integrated circuits, where the horizontal metal conductors 116 (e.g., in FIG. IE) are formed in recesses in the interlayer dielectric using chemical mechanical polishing. After polishing, the next layers of vias (vertical interconnects) is formed on top and next to the interconnect layer. Thus any pattern-

ing of interconnects (to obtain patterned metal underlayers) should be done before the manufacturing of the next layer of vias.

[0011] With the methods disclosed in U.S. Patent No. 6,982,519, it is not possible to grow nanostructures directly on an insulating substrate such that the substrate will remain insulating, as there will be metal remaining in between the nanostructures after lithography. In some applications, it is desirable to have the nanostructure-covered surface insulating (e.g., growing nanostructures on the insulating surface 110 in FIG. 1C), for example, in heat transport from insulators (where a continuous metal layer is unwanted).

[0012] Furthermore, it is inconvenient to grow nanostructures on existing metal islands (such as that shown in FIG. ID), and the problem is exemplified by the plasma-induced chip damage as shown in the SEM picture in FIG. 2.

[0013] The configuration shown in FIG. 1E includes vias 118 (vertical interconnects) to some underlying (or overlying depending on the way the device is oriented) patterned metal underlayer 116. It would be preferable to grow nanostructures directly on the patterned metal underlayer 116 (horizontal interconnects) or any existing traditional-type vias 118 (vertical interconnects).

[0014] Another problem not addressed by U.S. Patent No. 6,982,519 is that not all metals used in the manufacturing of integrated circuits are compatible with the plasma gases used for growth of nanostructures. For example, U.S. Application Publication No. 2008/00014443 states that it is not possible to use copper in an acetylene-containing plasma as there will be a detrimental chemical reaction.

[0015] U.S. Application Publication No. 2007/0154623 discloses a method for using a buffer layer between a glass substrate and the catalyst to prevent interaction. U.S. Application Publication No. 2007/0259128 discloses a method for using an interlayer to control the site density of carbon nanotubes. Neither of these applications fulfills the need for nanostructure growth on already patterned metal underlayers, or for arc elimination.

[0016] When growing nanostructures on a chip only partially covered by a metal underlayer, there is sometimes a parasitic growth outside the catalyst particles. This can cause unwanted leakage currents along the chip surface.

[0017] Therefore, there is a need of a method to grow the nanostructures on a previously patterned metal underlayer without having the problems of arc-induced chip damage and overvoltage damage of sensitive electronic devices, or problems due to incompatibility of materials used, parasitic growth during plasma growth processing. In various implementations, the technology described herein can solve some or all of these processing-related problems.

[0018] The discussion of the background to the invention herein is included to explain the context of the invention. This is not to be taken as an admission that all materials referred to was published, known, or part of the common general knowledge as at the priority date of any of the claims.

[0019] US 2002/0167375 relates to a tunable nanomechanical resonator system comprising an nanofilter array. The nanofilter array may be formed by coating a substrate with a metal film, anodizing the metal to form pores in an ordered nanopore array, depositing catalytic material in the bottom of the pores, growing nanotubes in the pores and thereafter partly etching away the anodized metal to partly expose the nanotubes.

[0020] US 2006/0148370 discloses a method of producing microstructures and a method of producing a mold.

[0021] US 2003/0052585 discloses a device with individually addressable carbon nanofibers on an insulating substrate.

[0022] US 6 146 227 discloses a system and method for manufacturing carbon nanotubes as functional elements of MEMS devices.

SUMMARY OF THE INVENTION

[0023] The scope of the invention is defined solely by the attached claims. The technology described herein is generally related to the field of chemical vapor deposition (CVD) of nanostructures, and more specifically to reduction or elimination of plasma-induced damages during growth processing of nanostructures, and enabling self-aligned growth of nanostructure on both conducting and insulating surfaces.

[0024] According to the invention, the layer of catalyst is patterned after it is deposited. In some implementations, the substrate additionally comprises a metal underlayer, co-extensive with its upper surface, and which is covered by the conducting helplayer. In some implementations, the metal underlayer is patterned. In some implementations, the metal underlayer comprises one or more metals selected from: Cu, Ti, W, Mo, Pt, Al, Au, Pd, P, Ni, and Fe. In some implementations, the metal underlayer comprises one or more conducting alloys selected from: TiN, WN, and AlN. In some implementations, the metal underlayer comprises one or more conducting polymers. According to the invention, the substrate is an insulator. In some implementations, the substrate comprises an insulator with at least one conducting layer on top. In some implementations, any of the depositing is carried out by a method selected from: evaporating, plating, sputtering, molecular beam epitaxy, pulsed laser depositing, CVD, and spin-coating. In some implementations, the one or more nanostructures comprises carbon, GaAs, ZnO, InP, InGaAs, GaN, InGaN, or Si. In some implementations, the one or more nanostructures include nanofibers, nanotubes, or nanowires. In some implementations, the conducting helplayer comprises a material selected from: a semiconductor, a conducting polymer, and an alloy. In some implementations, the conducting helplayer is from 1 nm to 100 microns thick. In some

implementations, the one or more nanostructures are grown in a plasma. In some implementations, the selective removal of the conducting helplayer is accomplished by etching. In some implementations, the etching is plasma dry etching. In some implementations, the etching is an electrochemical etching. In some implementations, the etching is photo chemical pyrolysis etching. In some implementations, the etching is pyrolysis etching. In some implementations, the method further includes depositing an additional layer between the conducting helplayer and the layer of catalyst.

[0025] The methods and devices may offer one or more of the following advantages.

[0026] In some implementations, the method allows growth of nanostructures on one or more pre-patterned metal underlayer(s) as well as electrically insulating substrates. The method can offer protection against arc damages to electrically sensitive devices contained in the substrates. Limitation on growth plasma containing gases that are incompatible with the metal underlayer(s) or insulating layer(s) can be eliminated.

[0027] The method comprises depositing a continuous electrically conducting helplayer covering a top surface of the substrate, then depositing (and/or patterning) a catalyst layer over the helplayer, growing the nanostructures on the catalyst layer, and then selectively removing the conducting helplayer in areas not covered by the nanostructures. The method can result in self-aligned fibers growing on the patterned catalyst-helplayer stack. A good grounding for the growth is achieved by the continuous conducting helplayer during the growth process, and it eliminates the arcing problem. Therefore, the method enables growing nanostructures on specifically designated locations on an already patterned metal underlayer(s) or insulating layer(s), as it is easy to remove the conducting helplayer after the nanostructures are grown.

[0028] Another advantage of the technology described herein is that sensitive electrical devices on the substrate are protected from the high voltages of the plasma, as all electrical connectors on the chip surface are shorted together and grounded. The technology described herein eliminates substantially all arcs, but even if there are some sparks (for example caused by static electricity during substrate handling) the damaging effect of the sparks is significantly reduced.

[0029] A third advantage is that the (possibly patterned) metal underlayer is protected from the plasma during the growth of the nanostructures. This is important when growing nanostructures on a metal underlayer(s) or insulating layer(s) that are not compatible with the gases used for the growth. For example, growth on a copper surface using an acetylene-containing plasma causes detrimental effects during nanostructure growth, as these materials are not always compatible. By utilizing the methods disclosed in this specification, such limitations on compatibility between plasma gases and substrates or metal underlayers can be eliminated.

[0030] A fourth advantage is that parasitic growth outside the catalyst is avoided.

[0031] As the removal of the conducting helplayer is a self-aligned process, individual nanostructures can be grown on or through an insulating layer/substrate that can remain insulating. This is accomplished by selectively removing the conducting helplayer so that the conducting helplayer material stays just underneath the nanstructures if the helplayer is deposited over the catalyst layer, or is completely removed if the helplayer is positioned on a layer other than the catalyst layer (such as an insultating layer deposited over the catalyst layer and the substrate). Other features and advantages will be apparent from the description and drawings and from the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032]

FIGS. 1A-1E illustrate example configurations not forming part of the invention for growing nanostructures on substrates.

FIG. 2A is an SEM (scanning electron microscope) image showing a spark-damaged chip surface.

FIGS. 3A-3E illustrate an example process for manufacturing the nanostructures in accordance with the invention.

FIGS. 4A-4B and 5A-5B show alternative embodiments of the invention.

FIG. 6 is a flow diagram of an example process for growing nanostructures on (partly) insulating surfaces.

FIGS. 7A-7B show an example optical waveguide structure not forming part of the invention.

FIGS. 8A-8B illustrate an example process for growing nanostructures through an insulating layer, not forming part of the invention.

FIGS. 9A-9B are SEM images showing an examplary device with a patterned metal underlayer, a continuous conducting helplayer and a patterned catalyst layer with grown nanofibers.

FIG. 10 is an SEM image showing the same examplary device with the helplayer selectively removed.

FIGS. 11A-11B are SEM images of examplary devices with copper as the underlayer, before and after the helplayer removal, respectively.

FIG. 12 is an SEM image of an examplary device where microstructures/nanostructures are grown through via holes in an insulating layer.

LIST OF REFERENCE NUMERALS USED HEREIN

[0033]

100 - conducting substrate
102 - catalyst layer, patterned to support growth of individual nanostructures
104 - catalyst layer, patterned to support growth of "forests" of nanostructures (multiple closely-spaced nanostructures)
106 - individual nanostructure
108 - "forest" of nanostructures (multiple closely-spaced nanostructures)
110 - insulating substrate
112 - continuous metal underlayer
114 - patterned metal underlayer on top of an insulator
116 - patterned metal underlayer having a top surface that is at the same level as the top surface of the insulating substrate (flat chip after polish)
118 - via (vertical interconnect)
120 - continuous conducting helplayer
122 - residuals of catalyst layer (after self-aligned etching)
124 - residuals of conducting helplayer (after self-aligned etching)
126 - optional layer
128 - substrate for waveguide
130 - waveguide material
132 - remaining vertical sidewalls of the conducting helplayer
134 - patterned conducting helplayer
136 - via hole through an insulator
200 - Depositing a conducting helplayer
210 - Depositing optional additional layers
220 - Depositing and patterning a catalyst layer
230 - Growing nanostructures
240 - Selective and self-aligned removal of helplayer

[0034] Like reference numbers and designations in the various drawings indicate like elements.

DETAILED DESCRIPTION OF THE INVENTION

[0035] The technology described herein relates to plasma processing, for example, growth of nanostructures (i.e., structures having at least one dimension in the order of nanometers). In some implementations, the technology also applies to processing of structures with feature sizes other than in the nanometer range, for example in the micrometer or millimeter size range.

[0036] "Substrate" is a designation of any layer or layers on which other layers can be deposited for the growth of nanostructures. Substrates can include semiconductors containing devices or metal layers or insulators. Semiconductors can include doped or undoped silicon, silicon carbide, II-VI or III-V materials (GaAs, InP, InGaAs etc) or semiconducting polymers. A substrate can also be transparent, conducting or insulating materials such as glass or indium-tin-oxide (ITO). A substrate can also include polymer layers or printed circuit boards (PCBs). A substrate does not need to be flat and can contain corrugated structures.

[0037] "Metal underlayer" can include any metal already present on the top surface of a substrate structure before the helplayer is deposited onto the substrate structure, including exposed metal islands (e.g., interconnects or vias) and/or continuous conducting layers that are disposed between the substrate and an exposed insulator layer on top. A metal underlayer can comprise any metal and/or metal alloy or combinations of different metals from the periodic table, such as Cu, Ti, W, Mo, Pt, Al, Au, Pd, Pt, Ni, Fe, etc. A metal underlayer can also comprise one or more conducting alloys such as TiN, WN, AlN. The metal underlayer can also comprise one or more conducting polymers. The metal underlayer can also comprise any combination of the above conducting materials.

[0038] "Catalyst" is a metal, alloy or material stack for promoting a chemical reaction. One example catalyst is silicon covered by nickel. The catalyst layer might also include a barrier layer, for example a tungsten layer deposited between a gold layer and the Si/Ni layer on top. A catalyst can be a pure metal such as Ni, Fe, Pt, Pd, or a metal alloy such as NiFe, NiCr, NiAlFe, etc.

[0039] "Insulator" can be any electrically insulating material such as silicon dioxide, silicon nitride or high-k materials such as HfO, ZrO, etc., aluminum oxide, sintered composites, polymers, resists (for example SU8), different forms of polyamide, ITO, so called low-k materials, or interlayer dielectrics (ILD).

[0040] "Deposited" means any one or more of evaporated, plated, sputtered, or deposited by chemical vapour deposition (CVD) such as thermal or plasma-enhanced CVD, by molecular beam epitaxy (MBE), by pulsed laser deposition (PLD), or by spin-coating.

[0041] "Nanostructure" is a structure that has at least one dimension in the order of nanometers. Nanostructures can include nanofibers, nanotubes or nanowires of carbon, GaAs, ZnO, InP, GaN, InGaN, InGaAs, Si, or other materials.

[0042] FIG. 3A shows a partly processed substrate such as a silicon chip. The technology described in this specification is applied to the insulating substrate 110 in order to grow nanostructures on the metal islands formed by interconnects 116 and vias 118 (patterned metal underlayer) embedded in the substrate. The vias 118 and interconnects 116 (patterned metal underlayers) can be manufactured according to standard wafer processing methods, for example, the so-called Damascene process, including etching trenches and depositing metals in the trenches. Chemical mechanical polishing (CMP) can be used to achieve a flat top surface of the substrate and interconnects.

[0043] To manufacture the structures shown in FIG. 3E, a number of steps are performed as shown in FIG.

6. First, a continuous conducting helplayer 120 is deposited (step 200) on the substrate 110 and the patterned metal underlayer 116 and 118 embedded in the substrate 110 to obtain the structure in FIG. 3B. Any electrically conducting material can be used as a helplayer 120. Examples of the conducting materials include any electrically conducting element from the periodic table of elements such as W, Mo etc., conducting alloys such as titanium nitride, semiconductors such as doped silicon, or conducting polymers. The material for the helplayer should be different from the material of the patterned metal underlayer unless a buffer layer separating the metal underlayer and the helplayer is first deposited. In the described example, a tungsten layer was employed as the continuous conducting helplayer 120.

[0044] The thickness of the conducting helplayer can be from about 1 nm to 100 μm, and preferably between about 1 nm and 100 nm. In one embodiment, a 50 nm layer of tungsten is used. In some embodiments, only one helplayer is used. However, the technology described herein is not limited to have only a helplayer with a single layer of material, the helplayer can also include multiple layers to improve lift-off, adhesion, etch selectivity or act as an etch stop layer, a seed layer for electroplating or a protection layer. Furthermore, layers for thermal management, for example layers with high or low thermal conductivity such as Peltier materials, can be included.

[0045] The technology described herein can be utilized with a number of different materials as the helplayer. It is important to select helplayer materials and etching parameters so that the nanostructures can be used as a self-aligned mask layer during the etching of the helplayer. The choice of the helplayer material can depend on the material lying beneath the helplayer. The helplayer can also be a catalyst, as the selective removal process can also be used to remove any unwanted catalyst residuals between the grown nanostructures.

[0046] The patterned catalyst layers 102 and/or 104 define where the nanostructures are to be grown. The catalyst can be nickel, iron, platinum, palladium, nickel-silicide, cobalt, molybdenum or alloys thereof, or can be combined with other materials (e.g., silicon). The catalyst can be optional, as the technology described herein can also be applied in a catalyst-free growth process for nanostructures. A patterned catalyst layer including a small catalyst dot 102 will give rise to an individual nanostructure, and a patterned catalyst layer including a large catalyst area 104 will give rise to a "forest" of nanostructures.

[0047] In order to pattern the catalyst layer (step 220 in FIG. 6), standard etch-back or lift-off processing with resist can be used. UV-light or an electron-beam can be used to pattern the resist layer. Other means can also be used to pattern the resist (or the catalyst directly), such as nanoimprint lithography or laser writing. The catalyst layer can also be patterned with methods that do not use a resist, for example, self-assembled chemical methods. An array of catalyst particles can be formed on the surface using Langmuir-Blodgett films, spinning on a solution with catalyst (nano-) particles onto the wafer or depositing a continuous catalyst film which is transformed to catalyst particles during annealing at elevated temperatures. Several of these techniques can be utilized to grow the catalyst layer on non-flat surfaces and to control the growth site density (number of growth sites per unit area).

[0048] During growth of the nanostructures, the conducting helplayer can be electrically grounded or connected to the potential of the substrate holder, or to some other suitable grounding potential. The nanostructures 106 and/or 108 can be grown in a plasma (step 230 in FIG. 6), typically a DC-plasma. The plasma gases used for nanostructure growth can be any carbon carrying precursor such as acetylene, carbon monoxide, methane, or higher order hydrocarbon, together with other gases such as ammonia, hydrogen, argon, or nitrogen. The growth temperature is preferably less than 800° C. A pressure ranging from about 0.1 to 250 Torr and preferably between about 0.1 to 100 Torr can be used. The plasma current can range from about 10 mA to 100 A, and preferably about 10 mA to 1 A.

[0049] In some implementations, RF-plasma or thermal CVD can be used to grow the nanostructures, and the technology described herein has applications especially for RF-plasmas with a DC-bias. In some implementations, the technology described herein also has application for nanostructures grown in gas-phase (without plasma) and in liquid phase.

[0050] In some implementations according to the technology described herein, after the growth step(s), the conductive helplayer is selectively removed by etching (step 240 in FIG. 6). The etching method and etch gases (for the case of dry etch) or etchants (for the case of wet etch) are chosen depending on the materials of the nanostructures and the conducting helplayer. For example, a helplayer comprising tungsten located under carbon nanofibers can be preferably removed by plasma dry etching using a fluorine-containing plasma. An advantage of this combination is the relative selectivity to the nanostructures and the catalyst particles.

[0051] Other etching methods, such as other anisotropic etch methods, wet (isotropic) etching, pyrolysis, electrochemical etching or photochemical etching, can be used. By using an etch-stop layer, or varying the etch time, a sufficiently strong etching can be carried out. It can be advantageous to choose an etchant or etch gas that has a relative selectivity between the conducting helplayer and the metal underlayer.

[0052] After the removal of the conducting helplayer 120 on specific locations using this self-aligned selective removal process, the final structure will consist of residuals of the conducting helplayer 122 below the residuals of the catalyst layer 124 and nanostructures 106 and/or 108 (see FIG. 3E).

[0053] With the method described herein, it is possible to manufacture individual nanostructures 106 or "forests"

of nanostructures 108 on isolated metal islands 116 or directly on the insulating substrate 110 as indicated in FIG. 3E.

[0054] It is also possible to form the nanostructures if the metal underlayer is not at the same level as the rest of the substrate. FIG. 4A illustrates isolated metal islands 114 deposited on top of an insulating substrate 110. The continuous conducting helplayer 120 is deposited over and covering the substrate surface (step 200), and then a patterned catalyst layer 102 and/or 104 is deposited (step 220) on the continuous conducting helplayer. After the growth of nanostructures (step 230) and the self-aligned selective removal (step 240) of the helplayer, the structure will appear as indicated in FIG. 4B.

[0055] In FIGS. 5A and 5B, a final structure formed by an alternative method is shown. First, the continuous conducting helplayer 120 is deposited throughout the top surface of the substrate (step 200), and then some optional patterned layer 126, for example to permit electrical conduction in the direction perpendicular to the nanostructures, is deposited (step 210) on the helplayer 120. Finally the patterned catalyst 102 and/or 104 is deposited (step 220) on the optional layer or the helplayer. After the growth process (step 230), the helplayer is selectively removed as described in a previous section (step 240). As with other methods described herein, no lithography is necessary after the nanostructure growth. Isolated islands (optional patterned layer 126) with nanostructures 106 and/or 108 on top, and residuals of the helplayer 124 below, are thus manufactured by the method illustrated by FIGS. 5A and 5B.

[0056] In another embodiment, not forming part of the invention, FIGS. 8A-8C illustrate the method of growing nanostructures through via holes created in an insulating material layer deposited on top of catalyst layer. First the catalyst layer 102 and/or 104 is deposited on a conducting substrate 100. The substrate in this case can however be an insulating substrate as well. An insulating layer 110 is then deposited on the substrate and the catalyst layer. A patterned conducting helplayer 134 is then deposited on top of the insulating layer 110. In some implementations, a continuous conducting helplayer can be deposited on top of the insulating layer first and then patterned by various suitable methods. Holes are then created by selectively etching the insulating layer 110 to create via holes 136 to the catalyst layer. Growth of nanostructures is then carried out to form nanostructures 106 and/or 108 on the catalyst layer 102 and/or 104. The patterned conducting helplayer 134 is then selectively removed (step 240 of FIG. 6), i.e., completely removed in this case.

[0057] If required, one of the materials below the conducting helplayer can be etched using an etchant with suitable relative selectivity. For example silicon oxide can be etched using wet or dry etching. Thus the catalyst and nanostructure layers are working as a mask for further processing.

EXAMPLES OF APPLICATIONS

[0058] An important application for the technology described in this specification is for making interconnects and/or thermal elevators in integrated circuits, which, for example, can be used in computing devices. The nanostructures are used to carry heat and electricity inside the integrated circuit chip or to/from the integrate circuit chip. The growth methods and devices used are compatible with current processing standards which involve patterning metals by polishing, and are also compatible with the metals involved. Also, 3-dimensional stacking of integrated circuits (several device layers) can utilize the nanostructures made with the methods described herein as interconnects. For example, a method is described in FIGS. 8A-8C to utilize the present invention to create via hole interconnect structures. FIG. 12 shows an SEM micrograph of a device where carbon nanostructures are grown through via holes in an oxide insulator as an exemplary device manufactured using the technology and methods described herein. In FIG. 12, the bright flat area is the insulating area and in the rest of the area, vertically grown nanostructures are visible.

[0059] Another application is the elimination of parasitic growth. When growing nanostructures on a chip that is only partially covered by a metal underlayer (i.e., by a patterned metal underlayer), there is sometimes a parasitic growth outside the catalyst particles. This can be avoided by using the continuous metal helplayer as described herein.

[0060] The technology described herein can also be used to protect the metal underlayer and other exposed materials from the plasma during the growth of nanostructures. This is particularly important when growing nanostructures on a metal underlayer that is not compatible with the gases used for the nanostructure growth. One example is nanostructure growth on a copper surface using acetylene-containing plasma, as copper and acetylene will react with each other. As the conducting helplayer can act as a diffusion barrier for oxygen or other materials of choice from reaching the metal underlayer, unwanted oxidation/chemical reaction/diffusion can be prevented. For example, an aluminum underlayer (if present) can be protected against oxidation by the helplayer. Furthermore, contaminants (for example metal ions) can also be reduced in the nanostructures produced using the method disclosed herein.

[0061] The technology described herein can also be used for protecting any sensitive electrical devices in the substrate from the high voltage arcs in the plasma during the nanostructure growth. If, after all, there are any arcs in the plasma, the resulting damage will be significantly reduced as all connectors on the substrate surface are shorted together and grounded by the conducting helplayer. This electrostatic discharge (ESD) protection is also important for handling a wafer in the laboratory or for shipping the partly finished wafer to another laboratory.

[0062] The methods described herein can also be used to manufacture thermal bumps on an insulating surface by means of self-aligned removal of the helplayer by plasma etching so that no metal is left except in areas just underneath the nanostructures.

[0063] The technology described herein can also be used to manufacture electrical conducting polymeric films and coatings while making the films optically partially transparent, transparent, or non-transparent. Applications can be, for example, making products such as electrode layers in displays, touch screens, electrostatic dissipation (ESD), and shielding etc.

[0064] Furthermore, the mechanical properties of the nanostructures created as described herein can be utilized to give mechanical stability to insulators, for example. It is then an advantage that no continuous metal underlayer is required, as the conducting helplayer is selectively removed by plasma etching (except just below the nanostructures) in a self-aligned process.

[0065] Thermal interface materials (TIMs), an example of anisotropic conducting films, can be manufactured using the technology described herein. In this case, a layer of nanostructures is embedded in a rubber of polymer designed to help increasing thermal conductivity. The polymer is first spun onto the nanofibers after the helplayer removal, and is then lifted off (with the nanostructures embedded therein). As there is no continuous metal film (since it has been selectively removed) below the polymer film, there is no risk of short-circuiting the different parallel nanostructures in the polymer film.

[0066] The conducting helplayer can also supply all nanostructures with the current necessary for electroplating, electrolessplating, or galvanic plating, if this is the next processing step to deposit a metal such as Au, Cu, Al, Ni, etc.

[0067] Another application is to make chemical probes directly onto partly insulating substrates. This can for example be done directly on a standard silicon integrated circuit.

[0068] The technology described herein can be used to manufacture source, drain and gate metal contact points for a transistor, such as CMOS, Bi-CMOS, Bi-polar, or HEMT etc. Variations of such configuration can be envisaged for particular transistor layouts. Applications also include devices with liquid crystals.

[0069] Some applications take advantage of the property that the helplayer can be removed in one-direction-only, if desired. Using anisotropic etch on an appropriately designed substrate structure will leave the helplayer on the vertical surfaces but remove it from the horizontal surfaces. As shown in FIG. 7A and 7B, a waveguide material 130 is deposited on a suitable substrate 128. The substrate 128 and the waveguide material 130 are covered by a helplayer 120 on the top surface as well as the side walls. By anisotropic etching, the helplayer on the top surface is selectively removed, leaving the side walls intact. As a result, a structure with individual nanofibers 106 grown on an otherwise transparent top surface and metallized sidewalls 132 is created. This structure is useful as an optical absorber for connecting the absorbed light into a waveguide 130 (which consists of the structure with helplayer coated side walls).

[0070] The technology described herein also provides a way to rework processing methods. This means that processed wafers can be reworked in case of processing problems/failure simply by removing the nanostructures by chemical mechanical polishing (CMP) to remove the nanostructures and start over the process.

[0071] The present technology is applicable for attaching technologies such as ball grid arrays (BGA), flip chip (FC) modules, CSP, WLP, FCOB, TCB etc., IC types, RFID tags, CMOS, BiCMOS, GaAS, HEMT AIGAAs, MMIC, MCM, LCD, displays, mobile handset, ASIC chips, memory devices, MCU, and integrated passive components etc.

EXEMPLARY DEVICES

[0072] In order to demonstrate the principle, a patterned gold (under-)layer (with a titanium adhesion-promotion layer below) was formed on an otherwise insulating oxide surface (using standard lithographic techniques). It is not desirable to put the catalyst directly on the patterned metal underlayer, as that would give rise to large plasma-induced damages during the growth. Instead, a tungsten helplayer (50 nm) was sputtered all over the chip surface. Then the patterned catalyst layer (Si 10 nm and Ni 10 nm) was formed (aligned with the patterned metal underlayer) by a standard lift off process. After growth, the structures appear as shown in FIGS. 9A and 9B. In this example, not forming part of the invention, the growth temperature was about 700 °C, and the plasma was generated in a mixture of C_2H_2 and NH_3 gases (20 and 100 sccm, respectively) at a pressure of about 4 Torr. The plasma current was set to 20 mA and the growth time was about 60 minutes. In this particular example, the catalyst was patterned such that a film ("forest") of nanofibers resulted after the growth process, but individual vertically aligned nanofibers will result if the catalyst regions are made smaller.

[0073] The conducting helplayer was then removed by plasma etching in a flourine-containing plasma (pressure 10 mTorr, gas flow 20 sccm CF_4), and using endpoint detection in a plasma etch CVD processing chamber.

[0074] The viability of the method can be shown by the SEM pictures taken before the processing (FIGS. 9A and 9B) and after the processing (FIG. 10). The fibers essentially look the same, despite the fact that the helplayer has been removed. Hence a self-aligned selective removal of the helplayer has been achieved, leaving only parts of the helplayer directly below the fibers remaining on the substrate. The complete removal of the helplayer from the rest of the areas was verified by electrical measurements. Minimal parasitic growth is seen outside the isolated metal island. A similar exemplary device with aluminum as the underlayer is shown in FIG. 11A, and

with copper as the underlayer in FIG. 11B, respectively.

[0075] Thus the goal of growing nanofibers on a patterned metal underlayer (on an otherwise insulating chip surface) has been achieved without plasma-induced chip damage.

[0076] FIG. 12 shows an SEM micrograph of an examplary device where carbon nanostructures are grown through via holes in an oxide insulator as an examplary device manufactured using the technology and methods described herein. In FIG. 12, the bright flat area is the insulating area and in the rest of the area, vertically grown nanostructures are visible. Thus the goal of growing nanofibers through via holes in an insulating layer is achieved.

[0077] While the instant specification contains many specific implementation details, these should not be construed as limitations on the scope of any invention or of what may be claimed, but rather as descriptions of features that may be specific to particular embodiments of particular inventions. Certain features that are described in this specification in the context of separate embodiments can also be implemented in combination in a single embodiment. Conversely, various features that are described in the context of a single embodiment can also be implemented in multiple embodiments separately or in any suitable subcombinations. Moreover, although features may be described herein as acting in certain combinations and even initially claimed as such, one or more features from a claimed combination can in some cases be excised from the combination, and the claimed combination may be directed to a subcombination or variation of a subcombination.

Claims

1. A method for making nanostructures, the method comprising:

   providing an insulating substrate (110) with one or more isolated metal islands (116) on top of or embedded in the surface of the substrate;
   depositing a continuous electrically conducting helplayer (120) over and covering the substrate surface and the one or more isolated metal islands;
   depositing a patterned layer of catalyst (102; 104) on the conducting helplayer (120) over the one or more isolated metal islands;
   growing the nanostructures (106; 108) on the layer of catalyst (102; 104); and
   selectively removing the electrically conducting helplayer between and around the nanostructures using the nanostructures (106; 108) as a self-aligned mask.

2. A method for making nanostructures, the method comprising:

   providing an insulating substrate (110);
   depositing a continuous electrically conducting helplayer (120) throughout the top surface of the substrate;
   depositing a patterned conductive layer (126) on the helplayer;
   depositing a patterned layer of catalyst (102; 104) on the patterned conductive layer;
   growing the nanostructures (106; 108) on the patterned layer of catalyst; and
   selectively removing the electrically conducting helplayer between and around the patterned conductive layer using the patterned conductive layer (126) as a self-aligned mask.

3. The method of claim 1, wherein said isolated metal islands are made in an electrically conducting metal underlayer,
   said electrically conducting helplayer being deposited to cover said metal underlayer.

4. The method of claim 3, wherein the metal underlayer is patterned into said isolated metal islands.

5. The method of claim 3, wherein said metal underlayer is made of a material that is different from said electrically conducting helplayer.

6. The method of claim 5, wherein said step of selectively removing the electrically conducting helplayer comprises the step of:
   etching using an etchant or etch gas that has a relative selectivity between said electrically conducting helplayer and said metal underlayer.

7. The method of claim 1 or 2, wherein the nanostructures comprise carbon, GaAs, ZnO, InP, InGaAs, GaN, InGaN, or Si.

8. The method of claim 1 or 2, wherein the conducting helplayer comprises a material selected from: a semiconductor, a conducting polymer, and an alloy.

9. The method of claim 1 or 2, wherein the selective removal of the electrically conducting helplayer is accomplished by etching.

10. The method of claim 3, further comprising the step of:
    depositing an additional buffer layer separating the electrically conducting helplayer and the metal underlayer.

11. A device obtainable by the method for making nanostructures of claim 1, comprising:

    an insulating substrate (110) with one or more isolated metal islands (116) on top of or embedded in the surface of the substrate;

one or more nanostructures (106) arranged on the one or more isolated metal islands;
residuals (124) of an electrically conducting helplayer (120) arranged between the substrate (110) and the nanostructures; and
residuals (122) of a patterned catalyst layer (102; 104) arranged between the residuals of the electrically conducting helplayer and the nanostructures, wherein the residuals of the catalyst layer are present only directly below the nanostructures,
wherein the residuals of the electrically conducting helplayer are present only directly below said residuals of the catalyst layer.

12. A device obtainable by the method for making nanostructures of claim 2, comprising:

an insulating substrate (110) with isolated metal islands on top the surface of the substrate;
one or more nanostructures (106) arranged on the isolated metal islands;
residuals of an electrically conducting helplayer (124) present only between the isolated metal islands (126) and the substrate (110);
residuals (122) of a patterned catalyst layer (102) between the isolated metal islands and the nanostructures arranged on the isolated metal islands, wherein said residuals of a patterned catalyst layer are present only directly below said nanostructures.

Patentansprüche

1. Verfahren zum Herstellen von Nanostrukturen, das Verfahren umfassend:

Vorsehen eines Isolationssubstrats (110) mit einer oder mehr isolierten Metallinseln (116) auf der Oberfläche des Substrats oder darin eingebettet;
Auftragen einer fortlaufenden, elektrisch leitenden Hilfsschicht (120) über der Substratoberfläche und der einen oder mehr isolierten Metallinseln und diese abdeckend;
Auftragen einer gemusterten Schicht eines Katalysators (102; 104) auf der leitenden Hilfsschicht (120) über der einen oder mehr isolierten Metallinseln;
Züchten der Nanostrukturen (106; 108) auf der Schicht des Katalysators (102; 104); und
selektives Entfernen der elektrisch leitenden Hilfsschicht zwischen den und um die Nanostrukturen unter Verwendung der Nanostrukturen (106; 108) als eine selbstausrichtende Maske.

2. Verfahren zum Herstellen von Nanostrukturen, das Verfahren umfassend:

Vorsehen eines Isolationssubstrats (110);
Auftragen einer fortlaufenden, elektrisch leitenden Hilfsschicht (120) über die obere Oberfläche des Substrats hinweg;
Auftragen einer gemusterten leitfähigen Schicht (126) auf der Hilfsschicht;
Auftragen einer gemusterten Schicht eines Katalysators (102; 104) auf der gemusterten leitfähigen Schicht;
Züchten der Nanostrukturen (106; 108) auf der gemusterten Schicht des Katalysators; und
selektives Entfernen der elektrisch leitenden Hilfsschicht zwischen der und um die gemusterte leitfähige Schicht unter Verwendung der gemusterten leitfähigen Schicht (126) als eine selbstausrichtende Maske.

3. Verfahren nach Anspruch 1, wobei die isolierten Metallinseln in einer elektrisch leitenden Metallunterschicht hergestellt werden,
wobei die elektrisch leitende Hilfsschicht zum Abdecken der Metallunterschicht aufgetragen wird.

4. Verfahren nach Anspruch 3, wobei die Metallunterschicht zu den isolierten Metallinseln gemustert wird.

5. Verfahren nach Anspruch 3, wobei die Metallunterschicht aus einem Material hergestellt wird, das sich von der elektrisch leitenden Hilfsschicht unterscheidet.

6. Verfahren nach Anspruch 5, wobei der Schritt des selektiven Entfernens der elektrisch leitenden Hilfsschicht den folgenden Schritt umfasst:
Ätzen unter Verwendung eines Ätzmittels oder Ätzgases, das eine relative Selektivität zwischen der elektrisch leitenden Hilfsschicht und der Metallunterschicht aufweist.

7. Verfahren nach Anspruch 1 oder 2, wobei die Nanostrukturen Kohlenstoff, GaAs, ZnO, InP, InGaAs, GaN, InGaN oder Si umfassen.

8. Verfahren nach Anspruch 1 oder 2, wobei die leitende Hilfsschicht ein Material umfasst, das ausgewählt ist aus: einem Halbleiter, einem leitenden Polymer und einer Legierung.

9. Verfahren nach Anspruch 1 oder 2, wobei die selektive Entfernung der elektrisch leitenden Hilfsschicht durch Ätzen ausgeführt wird.

10. Verfahren nach Anspruch 3, ferner umfassend den folgenden Schritt:
Auftragen einer zusätzlichen Pufferschicht, die die

elektrisch leitende Hilfsschicht und die Metallunterschicht trennt.

11. Vorrichtung, die durch das Verfahren zum Herstellen von Nanostrukturen nach Anspruch 1 erzielbar ist, umfassend:

ein Isolationssubstrat (110) mit einer oder mehr isolierten Metallinseln (116) auf der Oberfläche des Substrats oder darin eingebettet;
eine oder mehr Nanostrukturen (106), die auf der einen oder mehr isolierten Metallinseln angeordnet sind;
Rückstände (124) einer elektrisch leitenden Hilfsschicht (120), die zwischen dem Substrat (110) und den Nanostrukturen angeordnet sind; und
Rückstände (122) einer gemusterten Katalysatorschicht (102; 104), die zwischen den Rückständen der elektrisch leitenden Hilfsschicht und den Nanostrukturen angeordnet sind,
wobei die Rückstände der Katalysatorschicht nur direkt unter den Nanostrukturen vorhanden sind,
wobei die Rückstände der elektrisch leitenden Hilfsschicht nur direkt unter den Rückständen der Katalysatorschicht vorhanden sind.

12. Vorrichtung, die durch das Verfahren zum Herstellen von Nanostrukturen nach Anspruch 2 erzielbar ist, umfassend:

ein Isolationssubstrat (110) mit isolierten Metallinseln auf der Oberfläche des Substrats;
eine oder mehr Nanostrukturen (106), die auf den isolierten Metallinseln angeordnet sind;
Rückstände einer elektrisch leitenden Hilfsschicht (124), die nur zwischen den isolierten Metallinseln (126) und dem Substrat (110) vorhanden sind;
Rückstände (122) einer gemusterten Katalysatorschicht (102) zwischen den isolierten Metallinseln und den Nanostrukturen, die auf den isolierten Metallinseln angeordnet sind,
wobei die Rückstände der Katalysatorschicht nur direkt unter den Nanostrukturen vorhanden sind.

Revendications

1. Procédé de fabrication de nanostructures, le procédé comprenant :

la fourniture d'un substrat isolant (110) avec une ou plusieurs îles métalliques isolées (116) sur la surface du substrat ou intégrées dans celle-ci ;
le dépôt d'une couche auxiliaire électroconductrice continue (120) par-dessus et recouvrant la surface de substrat et lesdites une ou plusieurs îles métalliques isolées ;
le dépôt d'une couche à motif de catalyseur (102 ; 104) sur la couche auxiliaire conductrice (120) par-dessus lesdites une ou plusieurs îles métalliques isolées ;
le développement des nanostructures (106 ; 108) sur la couche de catalyseur (102 ; 104) ; et
l'élimination sélective de la couche auxiliaire électroconductrice entre les nanostructures et autour de celles-ci en utilisant les nanostructures (106 ; 108) comme un masque auto-aligné.

2. Procédé de fabrication de nanostructures, le procédé comprenant :

la fourniture d'un substrat isolant (110) ;
le dépôt d'une couche auxiliaire électroconductrice continue (120) sur toute la surface supérieure du substrat ;
le dépôt d'une couche conductrice à motif (126) sur la couche auxiliaire ;
le dépôt d'une couche à motif de catalyseur (102 ; 104) sur la couche conductrice à motif ;
le développement des nanostructures (106 ; 108) sur la couche à motif de catalyseur ; et
l'élimination sélective de la couche auxiliaire électroconductrice entre la couche conductrice à motif et autour de celle-ci en utilisant la couche conductrice à motif (126) comme un masque auto-aligné.

3. Procédé selon la revendication 1, dans lequel lesdites îles métalliques isolées sont créées dans une sous-couche métallique électroconductrice,
ladite couche auxiliaire électroconductrice étant déposée pour recouvrir ladite sous-couche métallique.

4. Procédé selon la revendication 3, dans lequel la sous-couche métallique présente un motif dans lesdites îles métalliques isolées.

5. Procédé selon la revendication 3, dans lequel ladite sous-couche métallique est constituée d'un matériau qui est différent de celui de ladite couche auxiliaire électroconductrice.

6. Procédé selon la revendication 5, dans lequel ladite étape d'élimination sélective de la couche auxiliaire électroconductrice comprend l'étape suivante :

décapage à l'aide d'un décapant ou d'un gaz d'attaque qui présente une sélectivité relative entre ladite couche auxiliaire électroconductrice et ladite sous-couche métallique.

7. Procédé selon la revendication 1 ou 2, dans lequel les nanostructures comprennent du carbone, du GaAs, du ZnO, de l'InP, du InGaAs, du GaN, de l'InGaN ou du Si.

8. Procédé selon la revendication 1 ou 2, dans lequel la couche auxiliaire conductrice comprend un matériau sélectionné parmi : un semi-conducteur, un polymère conducteur et un alliage.

9. Procédé selon la revendication 1 ou 2, dans lequel l'élimination sélective de la couche auxiliaire électroconductrice est accomplie par décapage.

10. Procédé selon la revendication 3, comprenant en outre l'étape suivante :
dépôt d'une couche tampon additionnelle qui sépare la couche auxiliaire électroconductrice de la sous-couche métallique.

11. Dispositif obtenable par le procédé de fabrication de nanostructures selon la revendication 1, comprenant :

un substrat isolant (110) avec une ou plusieurs îles métalliques isolées (116) sur la surface du substrat ou intégrées dans celle-ci ;
une ou plusieurs nanostructures (106) agencées sur lesdites une ou plusieurs îles métalliques isolées ;
des résidus (124) d'une couche auxiliaire électroconductrice (120) agencée entre le substrat (110) et les nanostructures ; et
des résidus (122) d'une couche de catalyseur à motif (102 ; 104) agencée entre les résidus de la couche auxiliaire électroconductrice et les nanostructures,
dans lequel les résidus de la couche de catalyseur ne sont présents que directement sous les nanostructures,
dans lequel les résidus de la couche auxiliaire électroconductrice ne sont présents que directement sous lesdits résidus de la couche de catalyseur.

12. Dispositif obtenable par le procédé de fabrication de nanostructures selon la revendication 2, comprenant :

un substrat isolant (110) avec des îles métalliques isolées sur la surface du substrat ;
une ou plusieurs nanostructures (106) agencées sur les îles métalliques isolées ;
des résidus d'une couche auxiliaire électroconductrice (124) présents uniquement entre les îles métalliques isolées (126) et le substrat (110) ;
des résidus (122) d'une couche de catalyseur à motif (102) entre les îles métalliques isolées et les nanostructures agencées sur les îles métalliques isolées,
dans lequel lesdits résidus d'une couche de catalyseur à motif ne sont présents que directement sous lesdites nanostructures.

FIG 1A

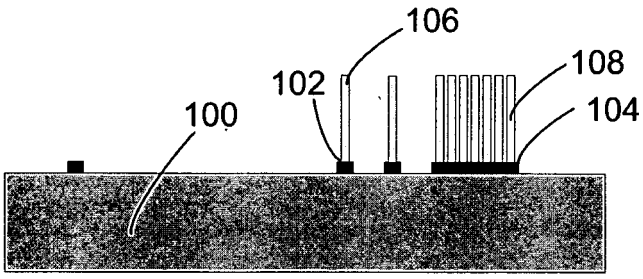


FIG 1B

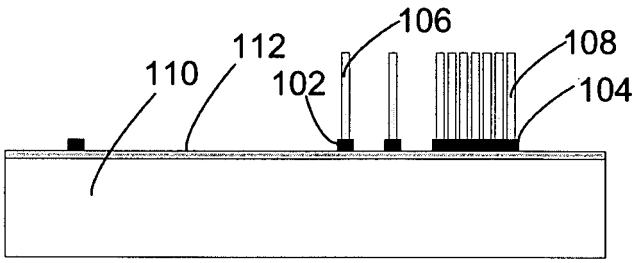


FIG 1C

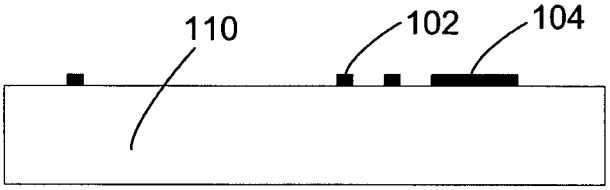


FIG 1D

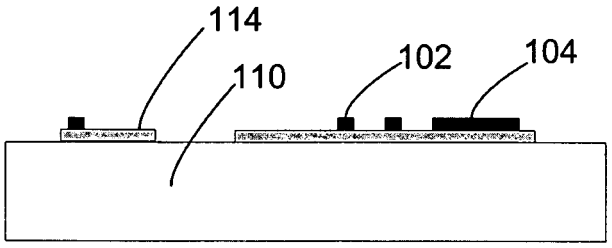


FIG 1E

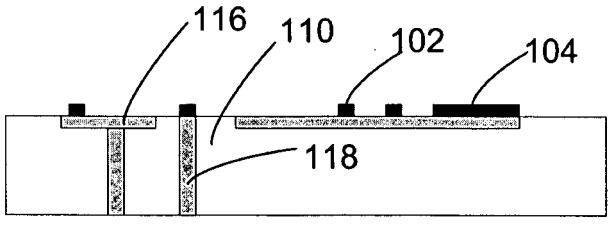


FIG. 2

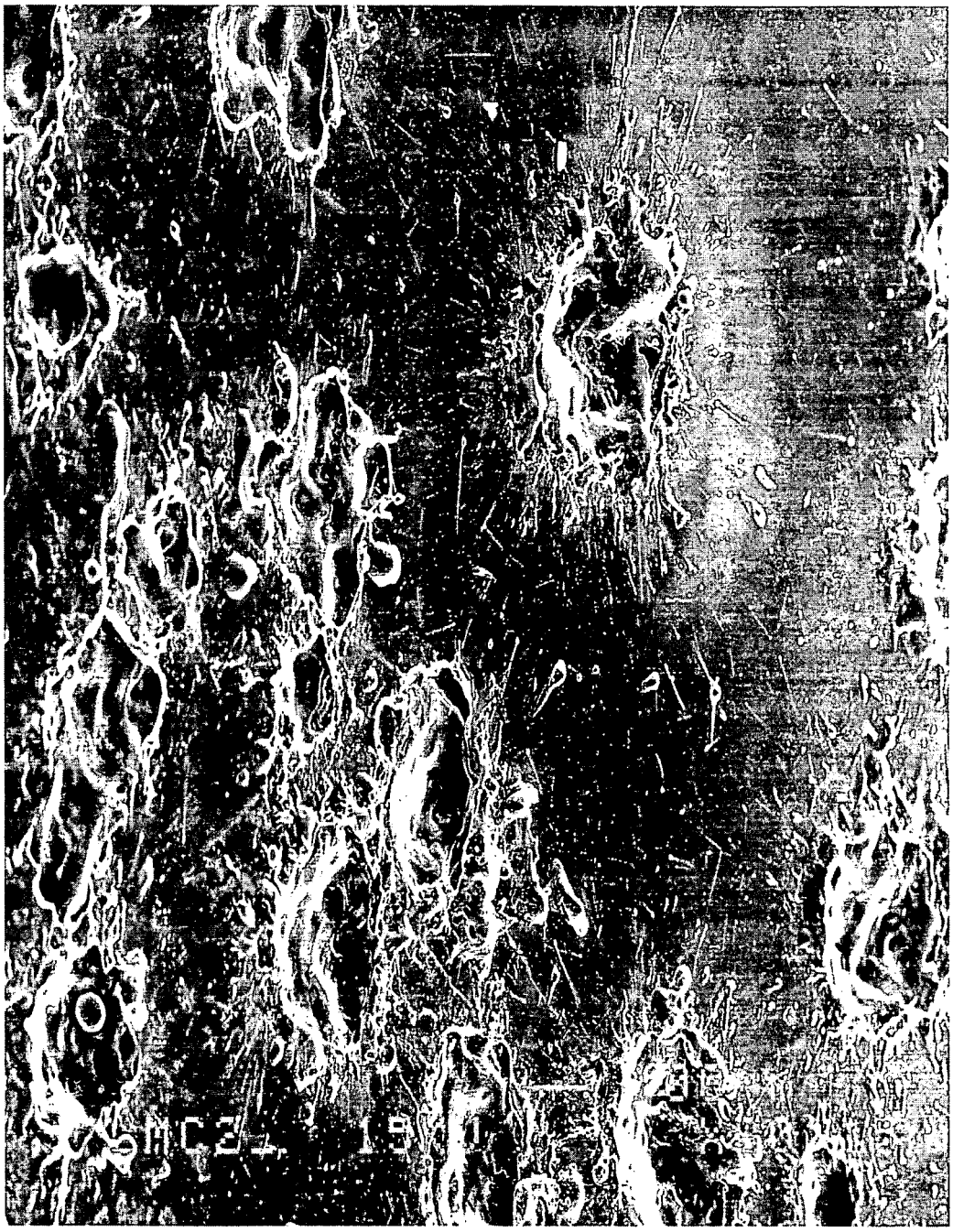


FIG 3A

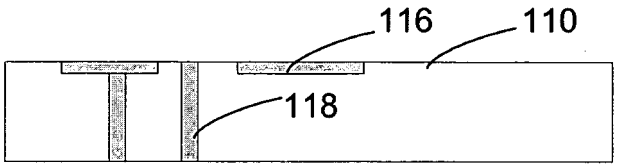


FIG 3B

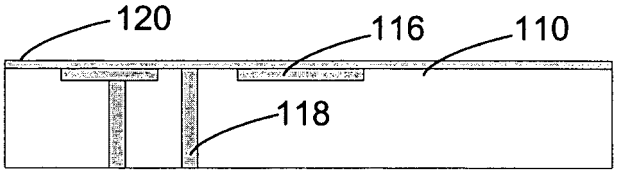


FIG 3C

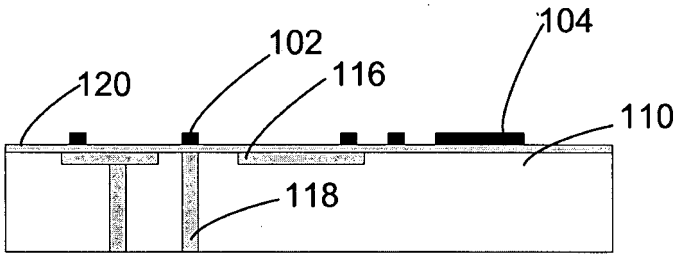


FIG 3D

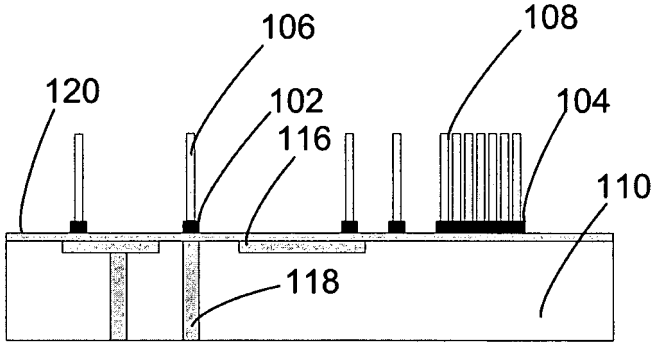


FIG 3E

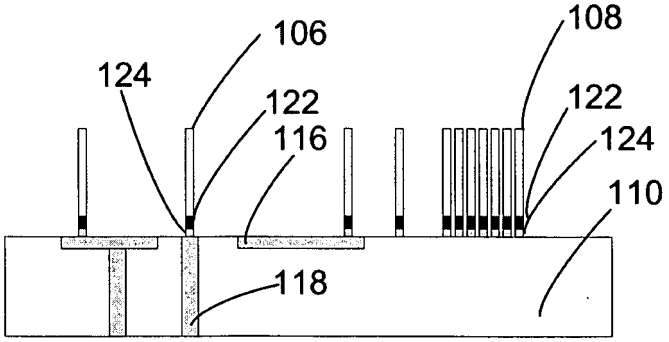


FIG 4A

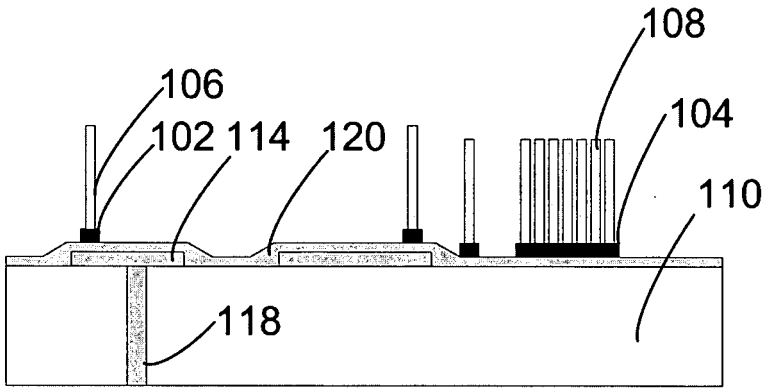
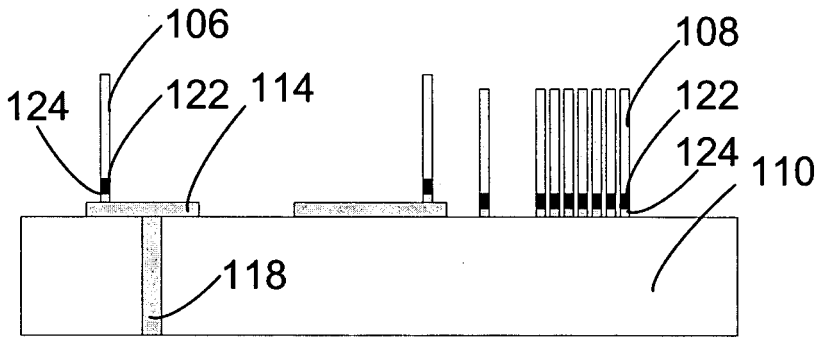

108
106
104
102
114
120
110
118

FIG 4B


106
108
124
122
114
122
124
110
118

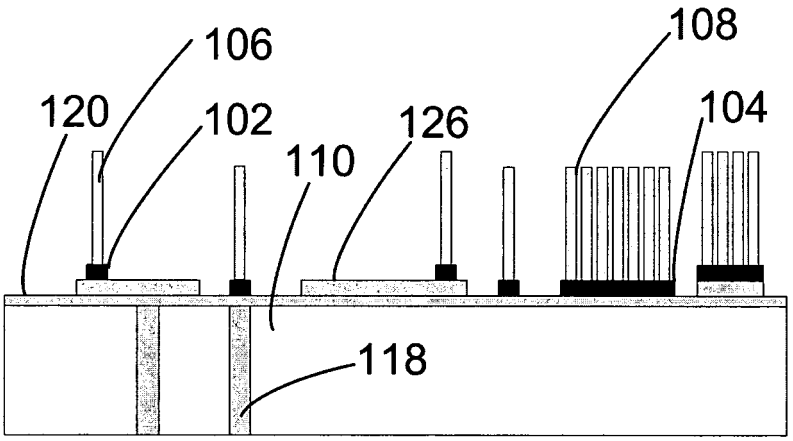

106
108
120
102
126
104
110
118

FIG 5A

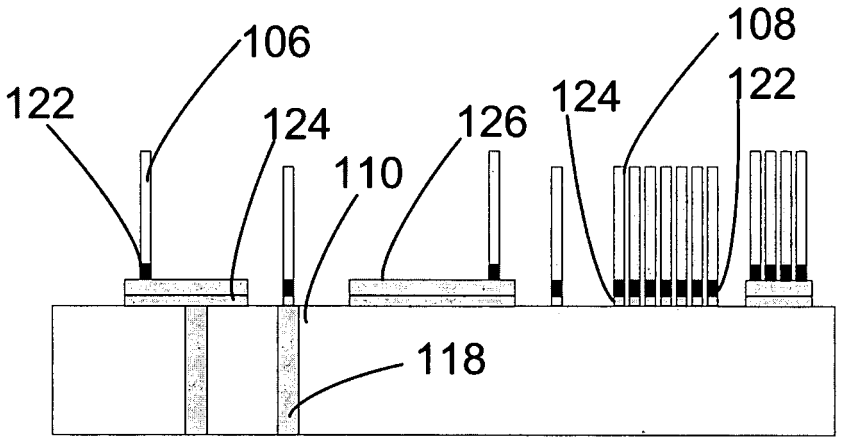
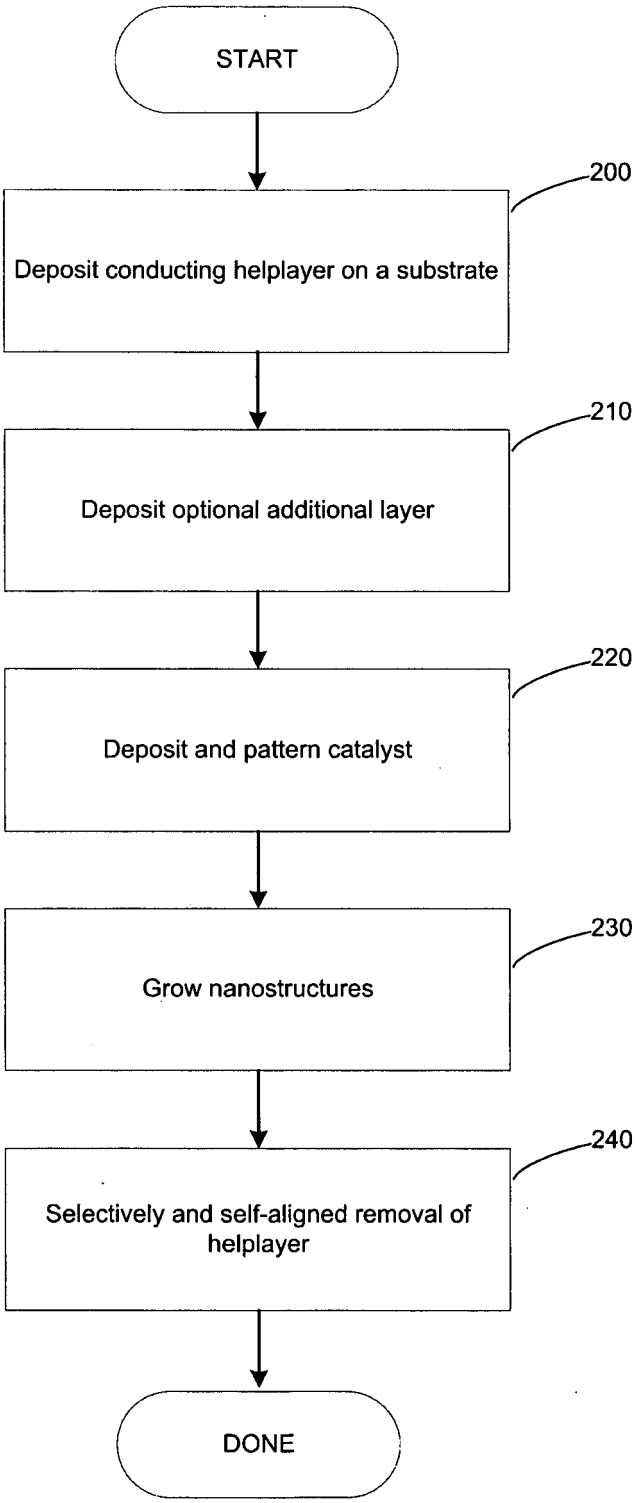
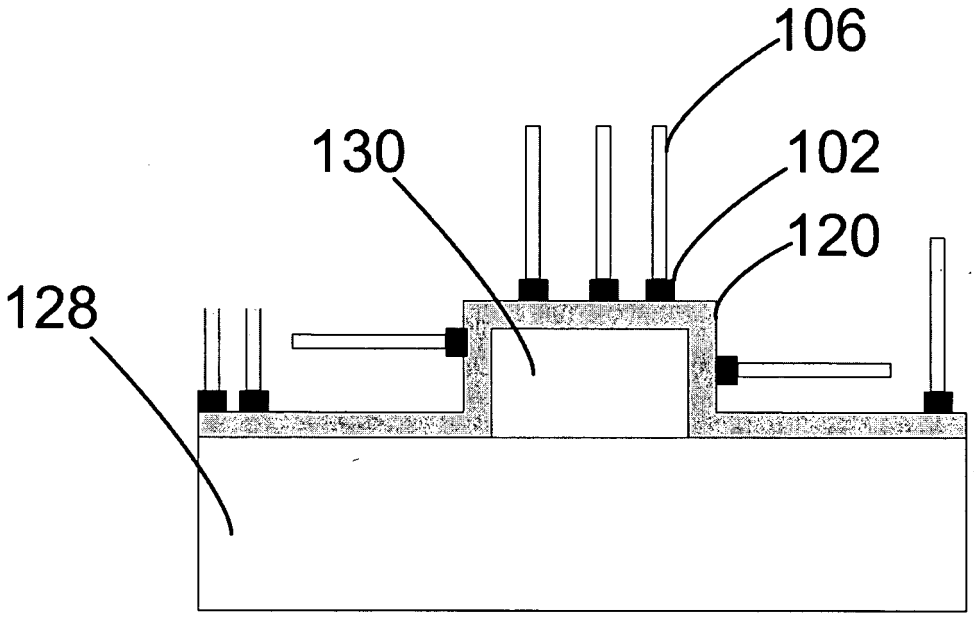

106
108
122
124
126
124
122
110
118

FIG 5B

FIG. 6


START
200
Deposit conducting helplayer on a substrate
210
Deposit optional additional layer
220
Deposit and pattern catalyst
230
Grow nanostructures
240
Selectively and self-aligned removal of helplayer
DONE

FIGs. 7A, 7B



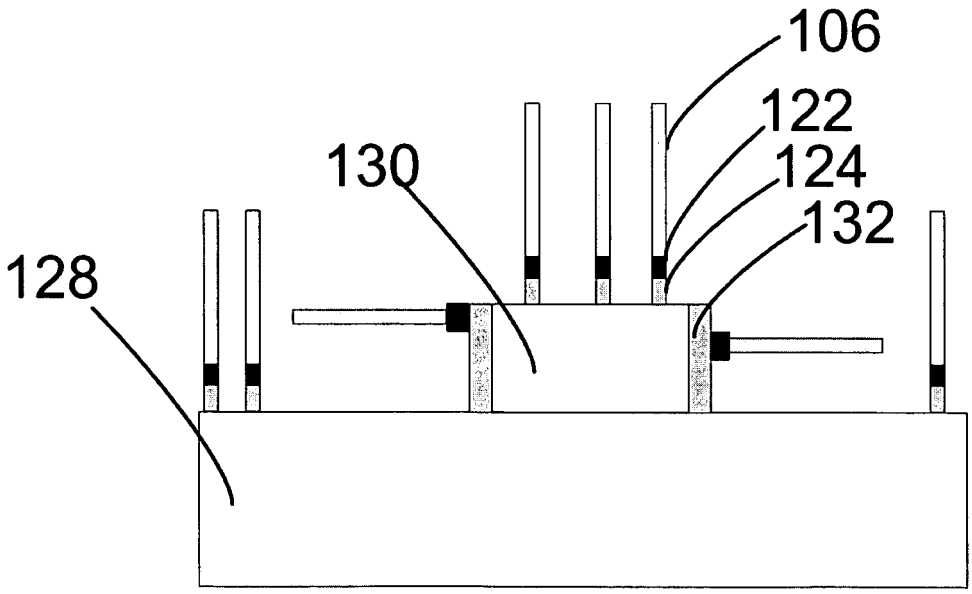


FIG 8A

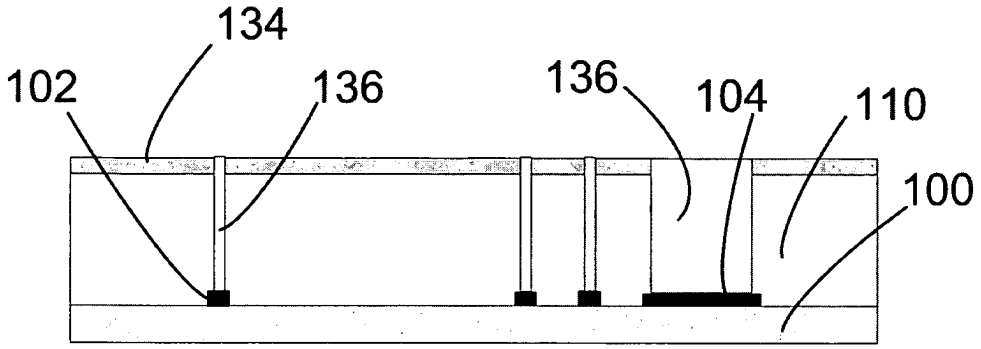


FIG 8B

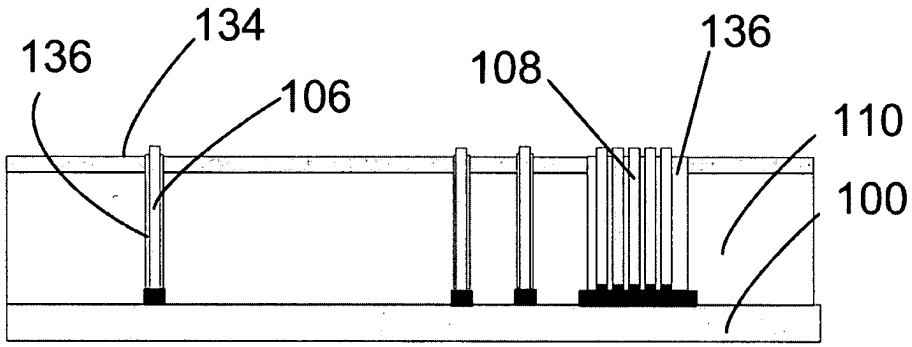


FIG 8C

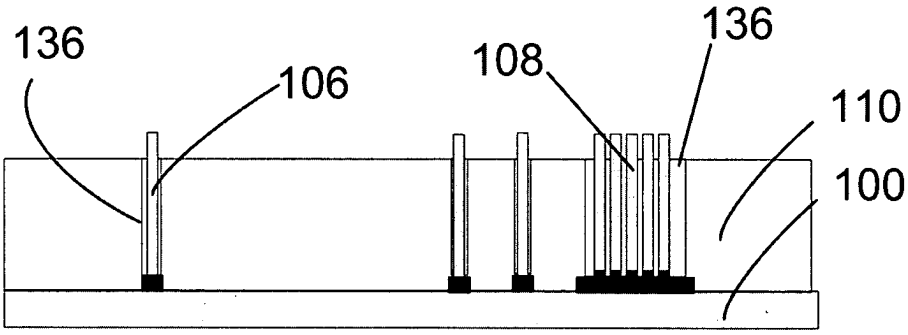


FIG. 9A

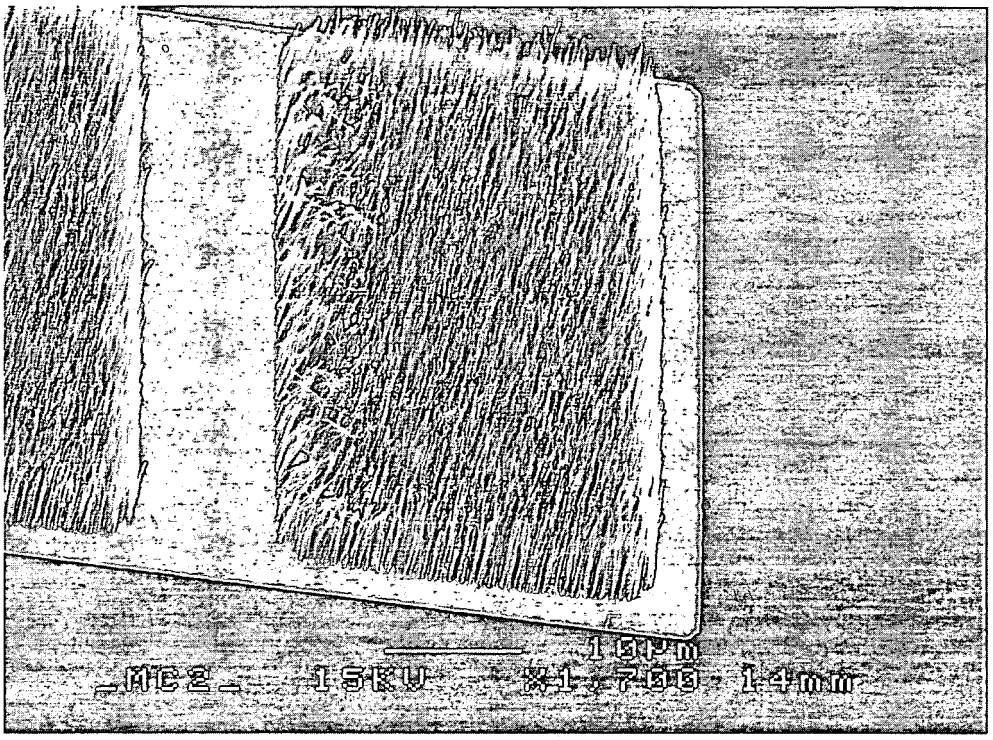


FIG. 9B

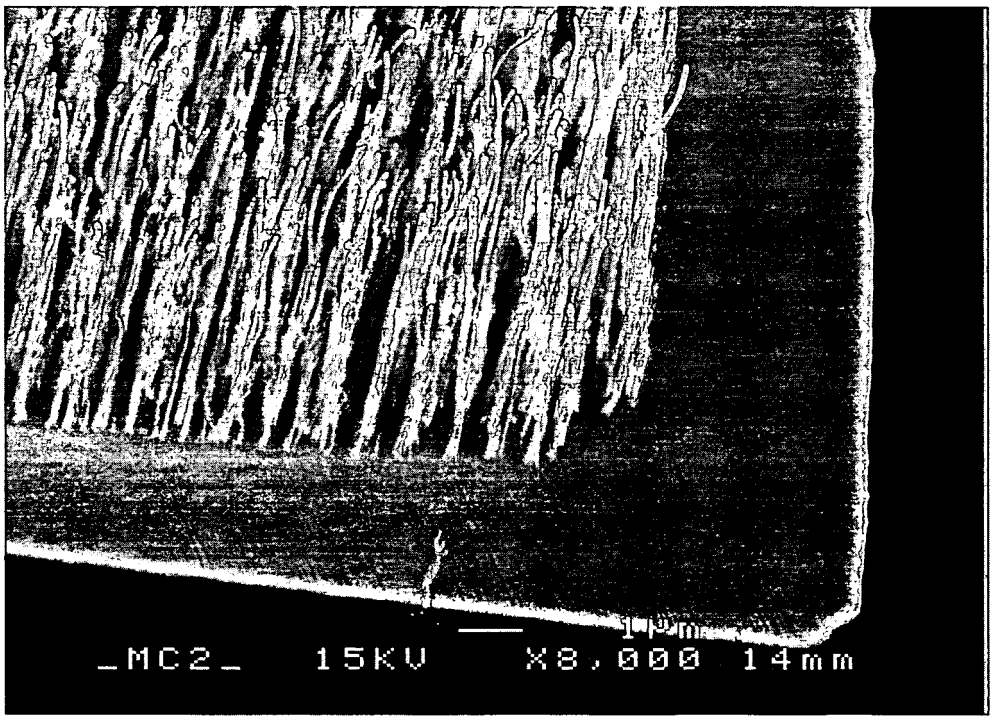


FIG. 10

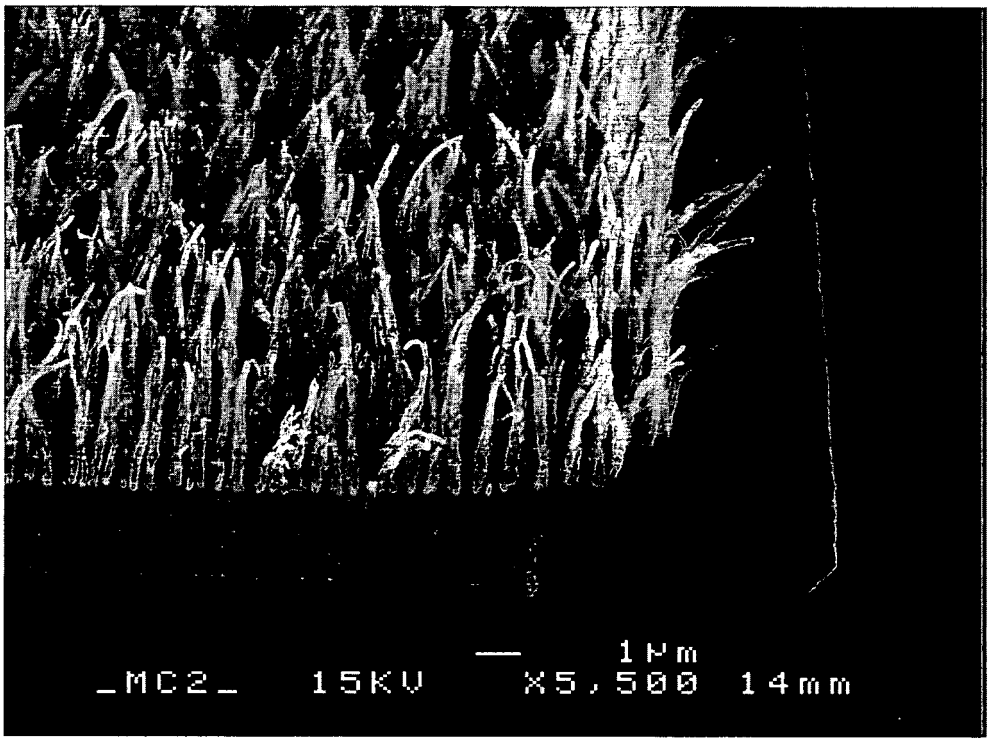


FIG. 11A

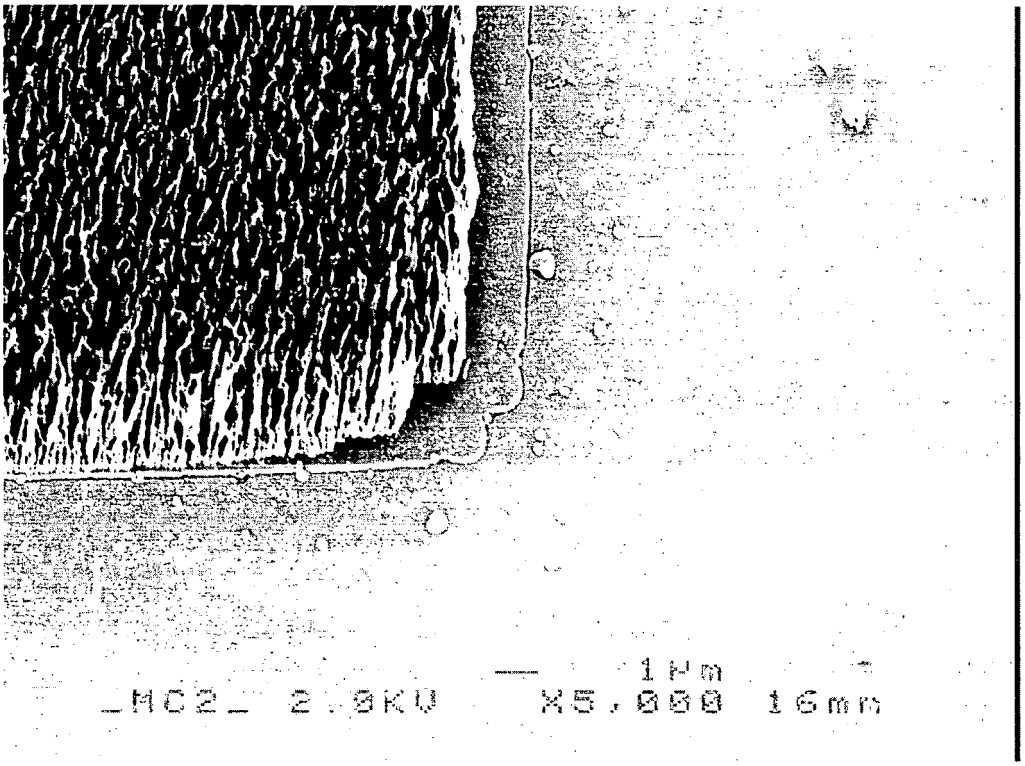


FIG. 11B

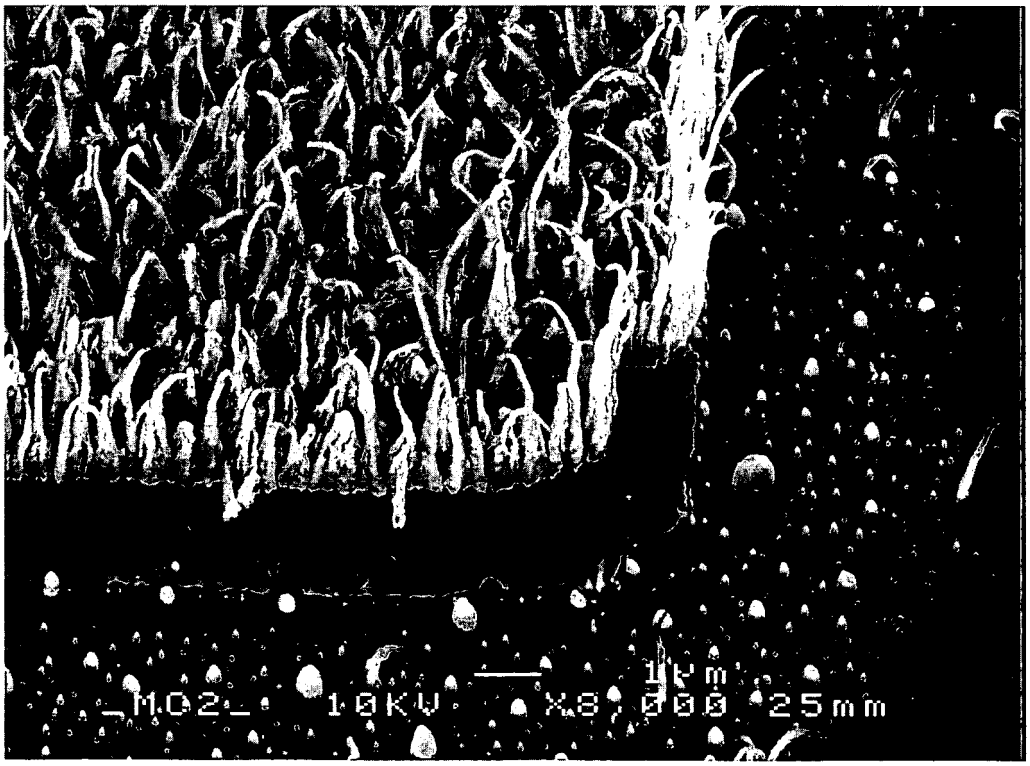
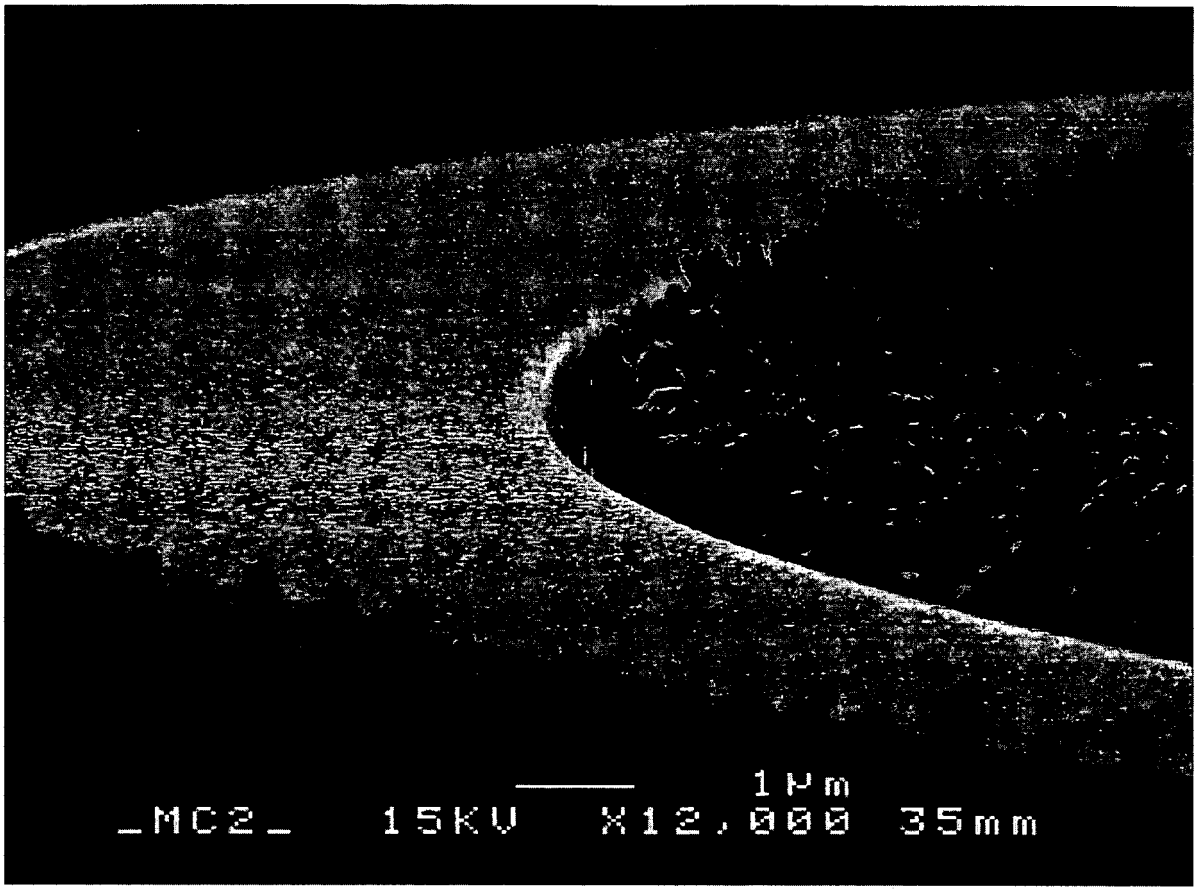


FIG. 12



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