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(54) **NANOSTRUCTURE DEVICE AND METHOD FOR MANUFACTURING NANOSTRUCTURES**

NANOSTRUKTURELEMENT UND VERFAHREN ZUR HERSTELLUNG VON NANOSTRUKTUREN

NANOSTRUCTURE ET PROCÉDÉ DE FABRICATION DE NANOSTRUCTURES

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Description

Field of the Invention

[0001] The present invention relates to a method of manufacturing nanostructures, and to a nanostructure device.

Technical Background

[0002] As the scaling of semiconductor devices continues into the nanometer regime there is an ever increasing search for new and improved nanostructures for replacing conventional devices and technologies. Many methods of fabricating nanostructures are known in the literature.

[0003] For example, US 7 687 876 discloses a method for fabricating nanostructures where several intermediate layers are deposited on a substrate followed by a catalyst layer from which nanostructures are grown. Through the provision of a multilayer stack between the substrate and the catalyst layer, the morphology as well as the electrical properties of the nanostructures can be tailored to a wide variety of applications. For certain applications, where such an extensive tailoring capability may not be required, it would be desirable to reduce the number of process steps involved in forming the nanostructures.

[0004] US 2008/0241493 discloses a substrate structure where TiN fine particles are deposited on a silicone substrate so that diameters of the TiN particles are about 3nm, and thereafter Co fine particles are deposited. The sizes of the Co fine particles are equal to or smaller than sizes of the TiN fine particles.

Summary of the Invention

[0005] In view of the above, it is an object of the present invention to provide an improved method for fabrication of nanostructures, and in particular a method for fabrication of nanostructures enabling cost reduction through reduced manufacturing complexity.

[0006] According to a first aspect of the present invention, it is therefore provided a method for manufacturing a plurality of nanostructures on a substrate, the method comprising: depositing a bottom layer on an upper surface of the substrate, the bottom layer comprising grains having a first average grain size; depositing a catalyst layer on an upper surface of the bottom layer, the catalyst layer comprising grains having a second average grain size larger than the first average grain size, thereby forming a stack of layers comprising the bottom layer and the catalyst layer; heating the stack of layers to a temperature where nanostructures can form and providing a gas comprising a reactant such that the reactant comes into contact with the catalyst layer.

[0007] The present invention is based on the realization that nanostructure growth can be promoted in a configuration with as few as two layers provided on a substrate by properly selecting the relation between the grain sizes of the layers provided on the substrate.

[0008] Two layers with different average grain size will give different mechanical properties of the layers, more specifically, the difference in average grain size will have an effect on the stress properties of the layers. The stress in a layer may in turn influence crystallographic properties and morphology. Here, the surface of the catalyst layer is altered in such a way that the surface properties of the catalyst layer promote nanostructure growth. Furthermore, a difference in grain size will enable interdiffusion between two adjacent layers. As interdiffusion may alter the crystallographic properties of the interdiffused layers, it may also lead to a change of stress in the layers thereby modifying crystallographic and morphological properties of the surface of the catalyst layer through recrystallization. The growth of nanostructures is influenced by both the crystallographic structure and morphology of the surface of the material from which they grow. Thus, by providing a bottom layer and a catalyst layer with different average grain sizes, conditions promoting growth of nanostructures using as few as two layers can be obtained, thereby achieving reduced manufacturing cost and process complexity.

[0009] The substrate may be made of any of a wide range of materials. Most commonly used are semiconductor-based materials such as silicon, silicon oxide, silicon nitride, silicon carbide, silicides, AlGaAs, AlGaN or SiGe but also other materials such as optically transparent substrates (ITO, quartz, glass, sapphire, diamond), polymers (polyimide, epoxies, PDMS, SU8, SAL6001) or any metals, metal alloys or insulators are possible.

[0010] As a bottom layer it is possible to use a wide range of insulating, semiconducting or conducting materials, and as a catalyst layer one may advantageously use metals or metal alloys such as Fe, Ni, NiCr, Au, Cu, Pt, Pd or Co. Additionally, it is also possible to use Co-based bimetals as a catalyst, examples of such bimetals are Co-V, Co-Fe, Co-Ni, Co-Pt, Co-Y, Co-Cu and Co-Sn.

[0011] Several different deposition methods are available for depositing the thin films of insulating, semiconducting or conducting materials used in the bottom and catalyst layers. Among the most common deposition methods are sputtering and different evaporation methods such as electron beam evaporation, thermal evaporation or resistive evaporation, but it is also possible to use other methods such as chemical vapor deposition (CVD) or electroplating, as long as such methods are tuned such that the desired different average grain sizes are achieved.

[0012] Henceforth, when discussing grain size it is always with reference to an average grain size. The average grain size can be measured using several different methods. One simple approach is to count the number of grains in a given area in a plane at the upper surface of a material or in a cross section, thereby calculating an average intersected grain area defining the average grain

size. Measuring the grain size area according to that method can advantageously be done by atomic force microscopy (AFM) or transmission electron microscopy (TEM).

[0013] In the context of the present application, the catalyst layer is a layer comprising a material or combination of materials acting as a catalyst in a catalytic process, wherein a chemical reaction between the catalyst and at least one reactant species takes place, leading to growth of nanostructures from the catalytic layer. A typical reaction in a catalytic process is the decomposition of organic compounds. In such a process the catalyst reacts with the organic compound, usually forming intermediate species that subsequently give the final reaction product from which the nanostructures are formed. The reactant may advantageously be provided in the form of a vapor, gas or as a component in a carrier gas. Growth of nanostructures may advantageously be performed by CVD methods such as Remote Plasma-Enhanced CVD (RPECVD), thermal CVD, Metal-Organic CVD (MOCVD), Plasma Enhanced CVD (PECVD), Microwave CVD, Inductively Coupled Plasma CVD (ICPCVD) or any other types of CVD known in the art.

[0014] In one embodiment of the present invention, the second average grain size may be at least 10% larger than the first average grain size.

[0015] In the present invention, the first average grain size (of the bottom layer) is smaller than the second average grain size (of the catalyst layer). Additionally, the bottom layer and the catalyst layer may advantageously have different material compositions.

[0016] As the diffusion at the interface between the bottom layer and the catalyst layer predominantly takes place along and around grain boundaries, having a smaller grain size in the bottom layer improves control of the diffusion process, thereby enabling better control of the crystallographic properties and morphology of the catalyst layer surface to promote nanostructure growth. For that reason, controlled diffusion by controlling the grain size of the different layers provides a greater degree of control of the catalyst layer.

[0017] Additionally, impurity elements may advantageously be introduced into at least one of the bottom layer and the catalyst layer during deposition of the layer(s), after deposition of one or both layers, or during nanostructure growth. Impurity elements may be introduced in gas phase, as reactive radicals, as ions, or in the form of vapor. Methods for introducing impurity elements may, for example, include annealing in an ambient gas containing impurity elements, and ion bombardment. Examples of such impurity elements include H, N, O, CO_2, Ar, H_2O vapor or combinations thereof. Impurity elements introduced during deposition of materials may change the growth kinetics of thin films which can result in additional stress, or impurities may change the grain size distributions in the deposited films, thereby affecting diffusion properties. Furthermore, introduction of impurity elements may also change the crystallographic structure of the material into which they are introduced, thus providing additional possibilities to tailor the grain size and diffusion properties.

[0018] There are several ways to control the relationship between the average grain size of the bottom layer and the average grain size of the catalyst layer. In general, a material deposited by sputtering will have a smaller grain size than a material deposited by evaporation. Therefore it may be advantageous to deposit one layer by sputtering and the other layer by evaporation to achieve a difference in grain size. As an example, different deposition methods may be used for forming the bottom layer and the catalyst layer to achieve different grain sizes.

[0019] In one embodiment of the present invention, the catalyst layer may be patterned prior to nanostructure growth, providing the option to only grow nanostructures in desired predefined positions.

[0020] According to a second aspect of the present invention, there is provided a nanostructure device, comprising: a substrate, a bottom layer arranged on an upper surface of the substrate, the bottom layer comprising grains having a first average grain size; a catalyst layer arranged on an upper surface of the bottom layer, the catalyst layer comprising grains having a second average grain size, larger than the first average grain size of the bottom layer, thereby forming a stack of layers; a plurality of nanostructures disposed on the catalyst layer wherein each of the nanostructures comprises: a base adjacent to the catalyst layer; a tip; and a body between the base and the tip.

[0021] Effects and features of this second aspect of the present invention are largely analogous to those described above in connection with the first aspect of the invention.

[0022] In one embodiment of the present invention, an interdiffused region where the two layers are mixed is present at the interface between the bottom layer and the catalyst layer. The interdiffused region can be distinguished by using measurement methods such as AFM or TEM or chemical analysis such as EDX or XPS.

[0023] According to one embodiment of the present invention, the bottom layer may advantageously be made of a first material selected from a group of materials having a relatively high melting point and the catalyst layer may advantageously be made of a second material, different from the first material, selected from a group of materials having a relatively low melting point, lower than the melting point of the first material. In general, layers formed from materials with lower melting points exhibit a larger average grain size than layers formed from materials with higher melting points. A material with a high melting point may advantageously be selected from the group of W, Mo or Ta and a material with a low melting point may be selected from the group of Fe, Ni, Au, Cu, Pt, Pd and Co.

[0024] In one embodiment of the present invention, the nanostructures may advantageously comprise carbon

and can for example be, carbon nanotubes or carbon nanofibers. Furthermore, a nanostructure may comprise a graphene layer.

[0025] It would also be possible to use the method of the present invention to fabricate nanostructure devices comprising nanostructures formed by semiconductor materials and/or metals such as InP, GaAs, InGaAs, GaN, SiC, Si, CdS, ZnO, TiO2, Ni, Al, Au, Ag, W, Cu, Pd, Pt, Mo or combinations thereof.

Brief Description of the Drawings

[0026] These and other aspects of the present invention will now be described in more detail with reference to the appended drawings showing a currently preferred embodiment of the invention, wherein:

Fig 1 schematically illustrates a nanostructure device according to an embodiment of the present invention;

Fig 2 is a flow-chart schematically illustrating a manufacturing method according to various embodiments of the present invention;

Figs 3a-d schematically illustrate the fabrication steps for making a nanostructure device;

Fig 4 schematically illustrates a single nanostructure from the nanostructure device in fig 1;

Fig 5 is a flow-chart schematically illustrating an embodiment of the method according to the present invention; and

Fig 6 is a flow-chart schematically illustrating another embodiment of the method according to the present invention.

Detailed Description of an Embodiment of the Invention

[0027] In the present detailed description, various embodiments of the method for manufacturing nanostructures according to the present invention are mainly discussed with reference to methods promoting controlled growth of nanostructures such as nanowires or nanofibres. Furthermore, the bottom layer and the catalyst layer are deposited using different deposition methods.

[0028] This should by no means be construed as limiting the scope of the present invention, which, for example, also encompasses methods and nanostructure devices where the nanostructures are made of other materials than carbon, and/or where the bottom layer and the catalyst layer are deposited using the same method.

[0029] Fig 1 schematically illustrates a nanostructure device 105 according to an embodiment of the present invention. Furthermore, Fig 1 shows the bottom layer 103 arranged on an upper surface of the substrate 102 and the catalyst layer 104 arranged on an upper surface of the bottom layer 103.

[0030] A method according to various embodiments of the present invention will now be described with reference to the flow-chart shown in Fig 2 outlining the general method steps for fabrication of nanostructures together with Figs 3a-d illustrating the nanostructure device in different stages of the manufacturing process.

[0031] In a first step 201, a suitable substrate 102 is provided as shown in Fig 3a. The substrate 102 can be of any insulating, semiconducting or conducting substrate, such as a silicon wafer of standard type.

[0032] In the next step 202, a conducting bottom layer 103 comprising a metal or metal alloy is deposited on the surface of the substrate 102 as illustrated in Fig 3b. The grain size of the bottom layer 103 is controlled through the choice of material and/or deposition method so as to produce a bottom layer having the desired average grain size. A bottom layer 103 having a relatively small grain size is achieved by using a material having a higher melting point and/or by depositing the material by sputtering.

[0033] Following the deposition of the bottom layer 103, the next step 203 is the deposition of a metallic catalyst layer 104 on top of the bottom layer 103, thereby forming a stack of layers as shown in Fig 3c. In order to achieve a difference in grain size between the bottom layer 103 and the catalyst layer 104, the process parameters governing the grain size of the catalyst layer 104 are determined with respect to the grain size of the bottom layer 103. A catalyst layer 104 having a larger grain size than the bottom layer 103 can be achieved by selecting a material with a lower melting point and/or depositing the material by evaporation. In Fig 3c it is more clearly illustrated that the grain size of the bottom layer 103 is smaller than the grain size of the catalyst layer 104.

[0034] The following step 204 comprises growth of the nanostructures 101. The growth process starts by heating the stack of layers in a step where the temperature is ramped up to a temperature suitable for nanostructure growth. As the stack of layers is heated, the bottom layer 103 and catalyst layer 104 interdiffuse at the interface between the two layers. The extension of the resulting interdiffused region 302 depends on material properties, temperature and time of exposure to an elevated temperature.

[0035] Additionally, it is also possible to alter the diffusion properties by introducing impurity elements into one or both of the layers. Impurities introduced during deposition of the layers may change the growth properties of the layers, thereby influencing stress properties and the resulting crystallographic structure. Impurities introduced during deposition may also alter the grain size as a result of dangling bonds and/or other defects. Alternatively, or in combination, impurities can be introduced by ion bombardment or annealing after the layers are grown, also altering the crystallographic properties of the surface so as to promote nanostructure growth.

[0036] When the sample is heated to the preferred temperature, a gas or vapor is provided containing the reactant species, which through a reaction with the catalytic layer 104 forms the nanostructures 101. Shown in Fig 3d is a nanostructure device 105 with a plurality of grown nanostructures 101.

Fig 3d also illustrates the interdiffused region 302 between the bottom layer 103 and the catalyst layer 104 as a region where the materials have merged and formed an alloy where distinctive grains no longer are discernible. However, atomic concentrations of both materials can be found in the interdiffused region 302 by using analysis methods such as energy-dispersive X-ray spectroscopy (EDX) or TEM.

[0037] The catalyst layer 104 may be patterned prior to nanostructure growth in order to manufacture nanostructures only in predefined locations. Alternatively, on a non-patterned surface, nanostructures grow from nucleation sites over the entire surface of the catalyst layer.

[0038] Fig 4 shows a schematic example of a single nanostructure 101. Each nanostructure 101 has a base 401 adjacent to the catalyst layer 104, a tip 403 and a body 402 between the base 401 and the tip 403. Due to the growth mechanisms of nanostructures, and of nanowires in particular, the tip 403 of the nanowires will have a cap-like formation as shown in Fig 4 containing material from the catalyst layer 104. Depending on the extension of the interdiffused region 302 between the two layers, there may also be traces of the bottom layer material 103 found in the tip 403 of the nanostructures 101.

EXAMPLES

[0039] The following examples are presented to further illustrate the invention and are not to be construed as unduly limiting the scope of this invention.

[0040] In a first example embodiment of the present invention illustrated by the flow chart in Fig 5, the first step 501 is to provide a substrate followed by the step 502 of depositing a bottom layer comprising W deposited by sputtering. Next, in step 503, a catalyst layer comprising Ni is deposited by evaporation. In the final step 504, carbon nanostructures are grown by PECVD using acetylene as a carbon carrying precursor.

[0041] In a second example embodiment of the present invention illustrated by the flow chart in Fig 6, the first step 601 is to provide a substrate followed by the step 602 of depositing a bottom layer comprising W deposited by sputtering. Next, in step 603, a catalyst layer comprising Pd is deposited by evaporation. In the next step 604, an impurity species in the form of H_2 is introduced into the fabrication process during temperature ramping stage prior to nanostructure growth. In the final step 605, carbon nanostructures are grown by PECVD. In this embodiment, methane is used as a carbon carrying precursor.

EXAMPLES OF APPLICATIONS

[0042] A possible application for the technology according to the present invention is for making interconnects in integrated circuits. Interconnects can be manufactured by first depositing a conductive bottom layer on the surface of a substrate where the bottom layer has a relatively small grain size. Next, a catalyst layer having a larger grain size is deposited, followed by growth of conductive nanostructures. The grown nanostructures are then covered by an insulating layer which is followed by an etching step to uncover the tip of the nanostructure. The exposed tip of the nanostructure is contacted by a conductive material to form the top contacts of an interconnect device.

[0043] Another application of nanostructures fabricated according to the present invention is for use in bump bonding where two conductive layers can be connected using a nanostructure assembly. The fabrication method is largely analogous to the method for fabricating interconnects. However, after exposing the nanostructure tips, the chip containing the device is flipped and contacted to a conductive surface on a second chip (flip chip bonding), thereby creating a connection between two conducting layers. Additionally, the surface exposing the nanostructure tips may be polished to achieve a uniform length of the nanostructures.

[0044] Using the bonding technology described above, it is also possible to use nanostructure devices as anisotropic conducting films (ACF). Yet another application is to use two devices as described above with exposed nanostructure tips to achieve Velcro bonding. This is done by pressing the two surfaces containing exposed tips against each other, thereby creating a bond between the two surfaces.

[0045] The methods described herein are applicable in general controlled growth of nanostrucutures. The methods may also be used in any assembly techniques for electronic components that include analog and/or digital electronic circuits. For example, such components may be found in: communications engineering, car/industrial electronics goods, consumer electronics, computing, digital signal processing and integrated products. Attaching technologies such as ball grid array (BGA), flip chip (FC) modules, CSP, WLP, FCOB, TCB, TSV 3D stacking, metallization schemes may utilize the methods herein. Integrated Circuit (IC) types such as RFID, CMOS, BiCMOS, GaAS, AlGAAs, MMIC, MCM, may utilize the methods described herein. Display technologies such as LCD's, LED's, and OLED's, as used in automobiles, computers, mobile phone handsets, and televisions may also incorporate nanostructures and connection techniques made by the methods described herein. Other electronic components that may similarly incorporate such technology include, but are not limited to: ASIC chips, memory devices, MCU, high frequency device modules, integrated passive components such as resistor, capacitors, inductors etc.

Claims

1. A method for manufacturing a plurality of nanostructures (101) on a substrate (102), the method comprising the steps of:

depositing a bottom layer (103) on an upper surface of the substrate (102), said bottom layer (103) comprising grains having a first average grain size;
depositing a catalyst layer (104) on an upper surface of the bottom layer (103), said catalyst layer (104) comprising grains having a second average grain size larger than said first average grain size, thereby forming a stack of layers comprising said bottom layer (103) and said catalyst layer (104);
heating the stack of layers to a temperature where nanostructures (101) can form; and
providing a gas comprising a reactant such that the reactant comes into contact with the catalyst layer (104).

2. The method according to claim 1, wherein the second average grain size is at least 10% larger than the first average grain size.

3. The method according to any one of the preceding claims, wherein the catalyst layer (104) has a first material composition and the bottom layer (103) has a second material composition that is different from said first material composition.

4. The method according to any one of the preceding claims, further comprising the step of:

introducing at least one impurity element into at least one of the bottom layer (103) and the catalyst layer (104) during deposition of said layers.

5. The method according to any one of claims 1 to 3, further comprising the step of:

introducing at least one impurity element into at least one of the bottom layer (103) and catalyst layer (104) after deposition of said layers.

6. The method according to any one of the preceding claims, further comprising the step of:

patterning said catalyst layer (104) prior to nanostructure growth.

7. The method according to any one of the preceding claims, wherein said bottom layer (103) is deposited by sputtering.

8. The method according to any one of the preceding claims, wherein said catalyst layer (104) is deposited by evaporation.

9. A nanostructure device (105), comprising:

a substrate (102);
a bottom layer (103) arranged on an upper surface of the substrate (102), said bottom layer (103) comprising grains having a first average grain size;
a catalyst layer (104) arranged on an upper surface of the bottom layer (103), said catalyst layer (104) comprising grains having a second average grain size, larger than the first average grain size of the bottom layer (103), thereby forming a stack of layers;
a plurality of nanostructures (101) arranged on said catalyst layer (104) wherein each of said nanostructures (101) comprises:

a base (401) adjacent to said catalytic layer (104);
a tip (403); and
a body (402) between said base (401) and said tip (403).

10. A nanostructure device (105) according to claim 9, wherein the bottom layer (103) and the catalyst layer (104) are interdiffused at the interface between said bottom layer (103) and said catalyst layer (104).

11. A nanostructure device (105) according to claim 9 or 10, wherein the catalyst layer (104) has a first material composition and the bottom layer (103) has a second material composition that is different from said first material composition.

12. A nanostructure device (105) according to any one of claim 9 to 11, wherein said tip (403) comprises material from said catalyst layer (104).

13. A nanostructure device (105) according to any one of claim 11 to 12, wherein the material of the bottom layer has a higher melting point than the material of the catalyst layer.

14. A nanostructure device (105) according to any one of claim 9 to 13, wherein said body (402) of said nanostructure (101) comprises carbon.

Patentansprüche

1. Verfahren zum Herstellen mehrerer Nanostrukturen (101) auf einem Substrat (102), wobei das Verfahren die folgenden Schritte umfasst:

Ablagern einer unteren Schicht (103) auf einer oberen Fläche des Substrats (102), wobei die untere Schicht (103) Körner mit einer ersten durchschnittlichen Korngröße aufweist;
Ablagern einer Katalysatorschicht (104) auf einer oberen Fläche der unteren Schicht (103), wobei die Katalysatorschicht (104) Körner mit

einer zweiten durchschnittlichen Korngröße umfasst, die größer als die erste durchschnittliche Korngröße ist, wodurch ein Schichtenstapel gebildet wird, welcher die untere Schicht (103) und die Katalysatorschicht (104) umfasst;
Erhitzen des Schichtenstapels auf eine Temperatur, bei der sich Nanostrukturen (101) bilden können; und
Bereitstellen eines Gases, umfassend einen Reaktanden, derart, dass der Reaktand in Kontakt mit der Katalysatorschicht (104) gelangt.

2. Verfahren nach Anspruch 1, wobei die zweite durchschnittliche Korngröße mindestens 10 % größer ist als die erste durchschnittliche Korngröße.

3. Verfahren nach einem der vorhergehenden Ansprüche, wobei die Katalysatorschicht (104) eine erste Materialzusammensetzung aufweist und die untere Schicht (103) eine zweite Materialzusammensetzung aufweist, die sich von der ersten Materialzusammensetzung unterscheidet.

4. Verfahren nach einem der vorhergehenden Ansprüche, ferner umfassend den Schritt:

Einführen von mindestens einem Verunreinigungselement in die untere Schicht (103) und/oder die Katalysatorschicht (104) während der Ablagerung der Schichten.

5. Verfahren nach einem der Ansprüche 1 bis 3, ferner umfassend den Schritt:

Einführen von mindestens einem Verunreinigungselement in die untere Schicht (103) und/oder die Katalysatorschicht (104) nach der Ablagerung der Schichten.

6. Verfahren nach einem der vorhergehenden Ansprüche, ferner umfassend den Schritt:

Bemustern der Katalysatorschicht (104) vor dem Wachstum der Nanostruktur.

7. Verfahren nach einem der vorhergehenden Ansprüche, wobei die untere Schicht (103) durch Aufdampfen abgelagert wird.

8. Verfahren nach einem der vorhergehenden Ansprüche, wobei die Katalysatorschicht (104) durch Verdunstung abgelagert wird.

9. Nanostrukturvorrichtung (105), umfassend:

ein Substrat (102);
eine untere Schicht (103), die auf einer oberen Fläche des Substrats (102) angeordnet ist, wobei die untere Schicht (103) Körner mit einer ersten durchschnittlichen Korngröße aufweist;
eine Katalysatorschicht (104), die auf einer oberen Fläche der unteren Schicht (103) abgelagert ist, wobei die Katalysatorschicht (104) Körner mit einer zweiten durchschnittlichen Korngröße umfasst, die größer als die erste durchschnittliche Korngröße der unteren Schicht (103) ist, wodurch ein Schichtenstapel gebildet wird;
mehrere Nanostrukturen (101), die auf der Katalysatorschicht (104) angeordnet sind, wobei jede der Nanostrukturen (101) umfasst:

eine Basis (401) benachbart zu der katalytischen Schicht (104):
eine Spitze (403) ; und
einen Körper (402) zwischen der Basis (401) und der Spitze (403).

10. Nanostrukturvorrichtung (105) nach Anspruch 9, wobei die untere Schicht (103) und die Katalysatorschicht (104) an der Kontaktfläche zwischen der unteren Schicht (103) und der Katalysatorschicht (104) interdiffundiert sind.

11. Nanostrukturvorrichtung (105) nach Anspruch 9 oder 10, wobei die Katalysatorschicht (104) eine erste Materialzusammensetzung aufweist und die untere Schicht (103) eine zweite Materialzusammensetzung aufweist, die sich von der ersten Materialzusammensetzung unterscheidet.

12. Nanostrukturvorrichtung (105) nach einem der Ansprüche 9 bis 11, wobei die Spitze (403) Material von der Katalysatorschicht (104) umfasst.

13. Nanostrukturvorrichtung (105) nach einem der Ansprüche 11 bis 12, wobei das Material der unteren Schicht einen höheren Schmelzpunkt als das Material der Katalysatorschicht aufweist.

14. Nanostrukturvorrichtung (105) nach einem der Ansprüche 9 bis 13, wobei der Körper (402) der Nanostruktur (101) Kohlenstoff umfasst.

Revendications

1. Procédé de fabrication d'une pluralité de nanostructures (101) sur un substrat (102), le procédé comprenant les étapes consistant à :

déposer une couche inférieure (103) sur une surface supérieure du substrat (102), ladite couche inférieure (103) comprenant des grains possédant une première taille de grains moyenne ;
déposer une couche de catalyseur (104) sur une surface supérieure de la couche inférieure

(103), ladite couche de catalyseur (104) comprenant des grains possédant une seconde taille de grains moyenne supérieure à ladite première taille de grains moyenne, formant ainsi un empilement de couches comprenant ladite couche inférieure (103) et ladite couche de catalyseur (104) ;
chauffer l'empilement de couches à une température à laquelle les nanostructures (101) peuvent se former ;
et
fournir un gaz comprenant un réactif tel que le réactif entre en contact avec la couche de catalyseur (104).

2. Procédé selon la revendication 1, dans lequel la seconde taille de grains moyenne est au moins 10 % supérieur à la première taille de grains moyenne.

3. Procédé selon l'une quelconque des revendications précédentes, dans lequel la couche de catalyseur (104) possède une première composition de matériau et la couche inférieure (103) possède une seconde composition de matériau qui est différente de ladite première composition de matériau.

4. Procédé selon l'une quelconque des revendications précédentes, comprenant en outre l'étape consistant à :

introduire au moins un élément d'impureté à l'intérieur d'au moins une de la couche inférieure (103) et de la couche catalyseur (104) pendant le dépôt desdites couches.

5. Procédé selon l'une quelconque des revendications 1 à 3, comprenant en outre l'étape consistant à :

introduire au moins un élément d'impureté à l'intérieur d'au moins une de la couche inférieure (103) et de la couche de catalyseur (104) après dépôt desdites couches.

6. Procédé selon l'une quelconque des revendications précédentes, comprenant en outre l'étape consistant à :

structurer ladite couche de catalyseur (104) avant la croissance des nanostructures.

7. Procédé selon l'une quelconque des revendications précédentes, dans lequel ladite couche inférieure (103) est déposée par pulvérisation.

8. Procédé selon l'une quelconque des revendications précédentes, dans lequel ladite couche de catalyseur (104) est déposée par évaporation.

9. Dispositif à nanostructures (105), comprenant :

un substrat (102) ;
une couche inférieure (103) agencée sur une surface supérieure du substrat (102), ladite couche inférieure (103) comprenant des grains possédant une première taille de grains moyenne ;
une couche de catalyseur (104) agencée sur une surface supérieure de la couche inférieure (103), ladite couche de catalyseur (104) comprenant des grains possédant une seconde taille de grains moyenne, supérieure à la première taille de grains moyenne de la couche inférieure (103), formant ainsi un empilement de couches ;
une pluralité de nanostructures (101) agencées sur ladite couche de catalyseur (104) dans laquelle chacune desdites nanostructures (101) comprend :

une base (401) adjacente à ladite couche catalytique (104) ;
une pointe (403) ; et
un corps (402) entre ladite base (401) et ladite pointe (403).

10. Dispositif à nanostructures (105) selon la revendication 9, dans lequel la couche inférieure (103) et la couche de catalyseur (104) sont interdifusées à l'interface de ladite couche inférieure (103) et de ladite couche de catalyseur (104).

11. Dispositif à nanostructures (105) selon la revendication 9 ou 10, dans lequel la couche de catalyseur (104) possède une première composition de matériau et la couche inférieure (103) possède une seconde composition de matériau qui est différente de ladite première composition de matériau.

12. Dispositif à nanostructures (105) selon l'une quelconque des revendications 9 à 11, dans lequel ladite pointe (403) comprend un matériau à partir de ladite couche de catalyseur (104).

13. Dispositif à nanostructures (105) selon l'une quelconque des revendications 11 à 12, dans lequel le matériau de la couche inférieure possède un point de fusion plus élevé que le matériau de la couche de catalyseur.

14. Dispositif à nanostructures (105) selon l'une quelconque des revendications 9 à 13, dans lequel ledit corps (402) de ladite nanostructure (101) comprend du carbone.

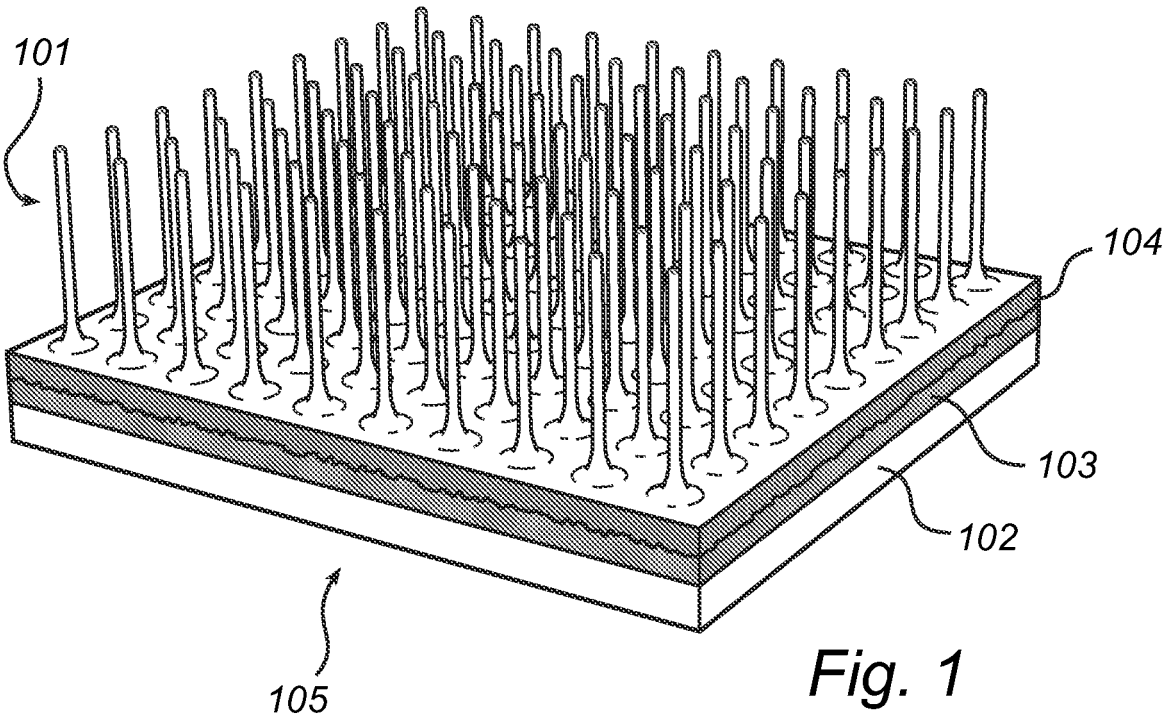

Fig. 1

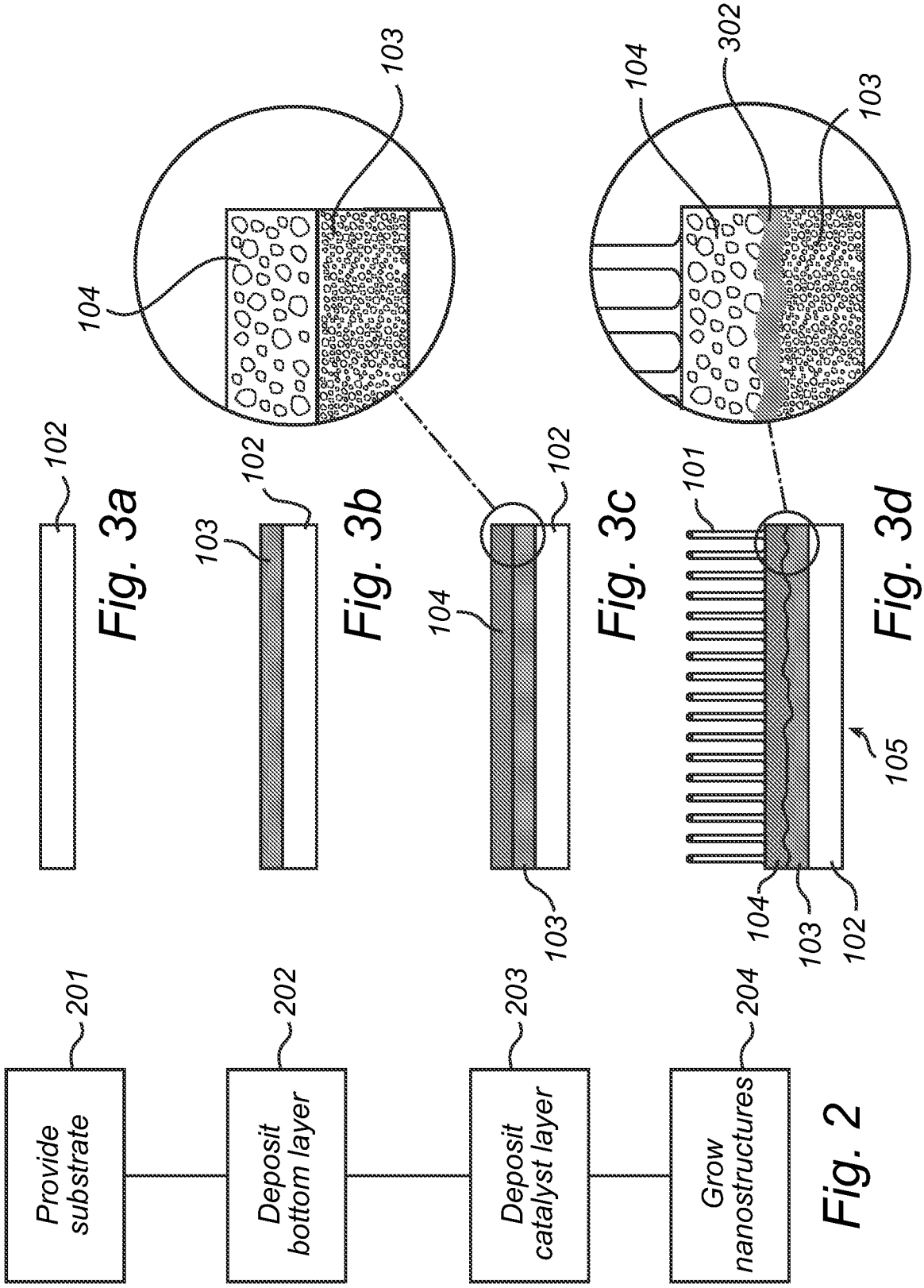

Fig. 3a

Fig. 3b

Fig. 3c

Fig. 3d

Fig. 2

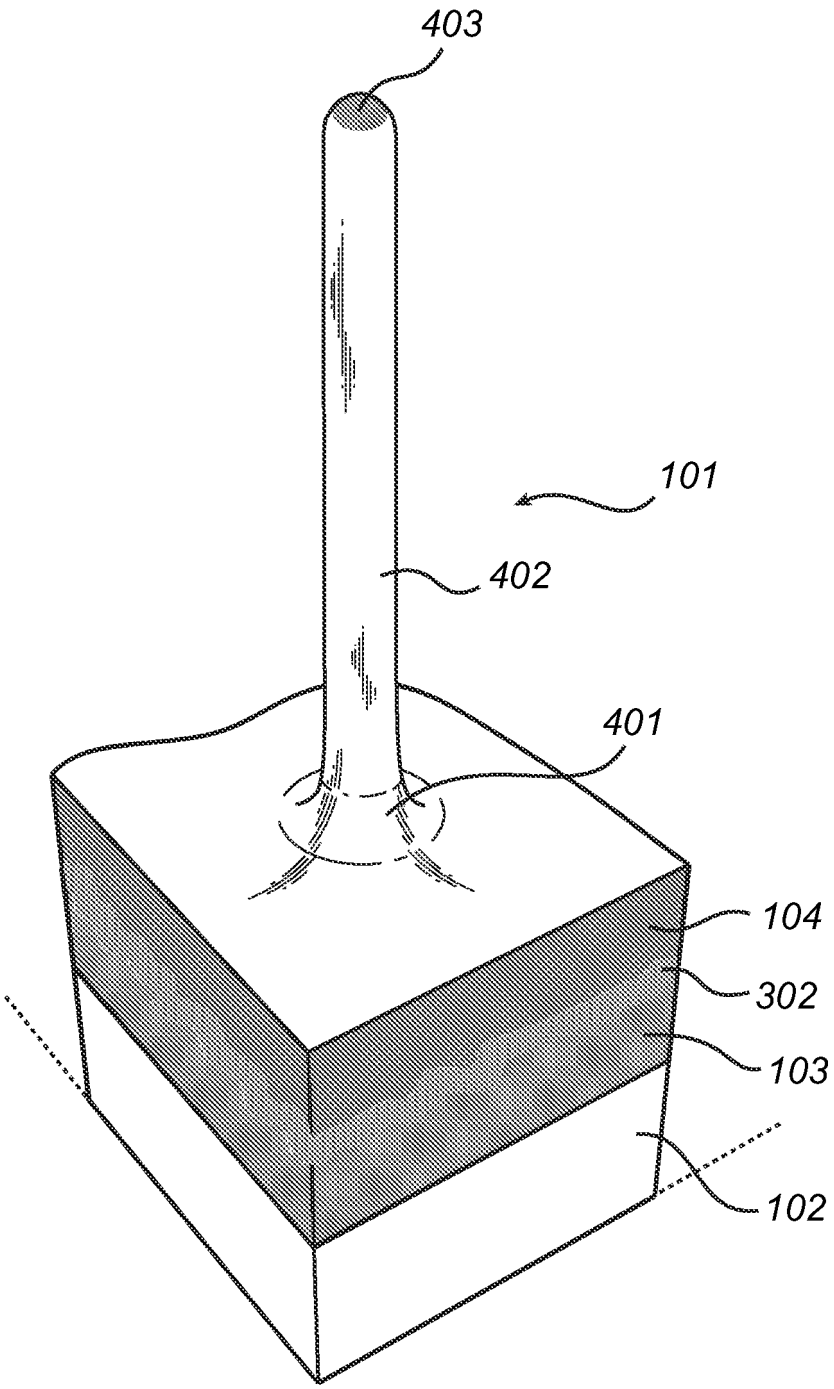

Fig. 4

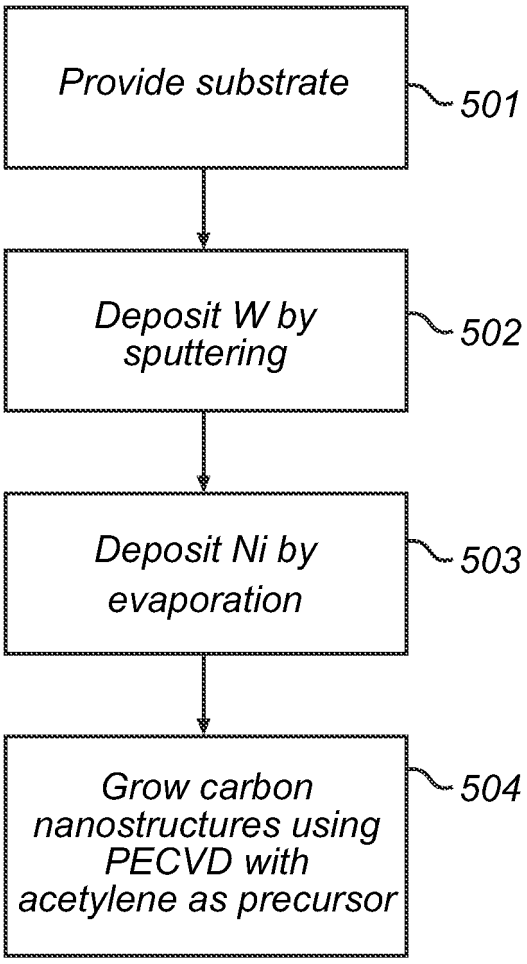
Provide substrate
501
Deposit W by sputtering
502
Deposit Ni by evaporation
503
Grow carbon nanostructures using PECVD with acetylene as precursor
504

Fig. 5

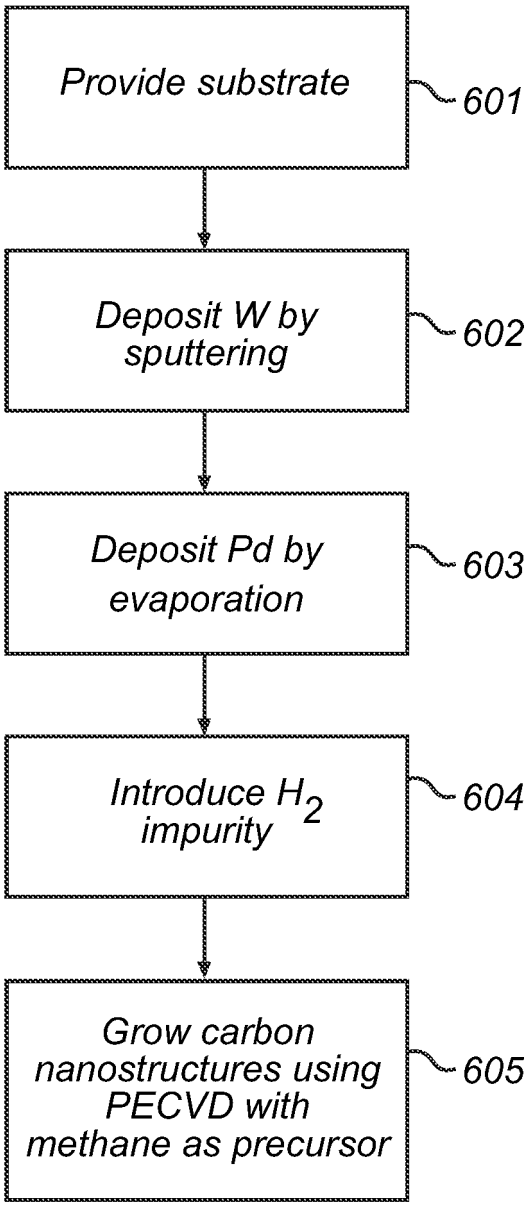
Provide substrate
601
Deposit W by sputtering
602
Deposit Pd by evaporation
603
Introduce H_2 impurity
604
Grow carbon nanostructures using PECVD with methane as precursor
605

Fig. 6

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 7687876 B **[0003]**
- US 20080241493 A **[0004]**